SAMSUNG ELECTRONICS

S6D0151X21

Rev. 1.00

MOBILE DISPLAY DRIVER IC

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http://www.samsung.com/Products/Semiconductor/DisplayDriverIC

IMPORTANT NOTICE!!

Precautions against Light

The conductivity of a semiconductor is strongly influenced by electro-magnetic radiation such as visible light, infrared light, ultraviolet light, or gamma radiation. When light is absorbed, electron-hole pairs are generated raising the conductivity of the material, eventually altering the electrical characteristics of the IC. Therefore, if the packages that expose IC's to external light sources, such as COB, COG, TCP and COF, are used, effective means to shield the IC from the light coming in all directions – top, bottom, and the sides – must be devised. Full observation of the following precautions is strongly recommended.

1. Make sure that the IC and substrate (board or glass) are protected from a stray light.
2. Always test and inspect products under the environment with no of light penetration.

Revision History

Version	Date	History
1.00	2008-05-06	Original

CONTENTS

FIGURES

TABLES

1. Introduction

1.1. Purpose of this document

This document has been created to provide a complete reference specification of S6D0151. IC design engineers would be referring to this specification to design the IC, and test engineers to test the compliance of the manufactured IC to guarantee the performance, and application engineers to assist the customers to make sure that they are using this IC properly.

S6D0151 is a single chip driver IC for a TFT-LCD panel. A source driver array with a built-in memory, gate drivers and power circuits are integrated onto the IC. It can drive a TFT-LCD panel to the maximum of 128-RGB x 160-dot graphics with 260k-color.

S6D0151 supports 18-/16-/9-/8-bits parallel bus interfaces and Serial Peripheral Interface (SPI). The IC also supports 18-/16-/6-bit RGB interface for motion picture display.

The active viewing area of the motion picture can be specified by Window Addressing Function. The specified window area can be updated selectively in order for motion picture image to be displayed independently and simultaneously with still picture display.

The IC features several power saving functions to reduce the overall power consumed in a TFT-LCD panel module: The IC operates at low voltage and has internal GRAMs that can store 128-RGB x 160-dot 260k-color image data to suppress unnecessary data transfers over the I/F's, saving overall power. In addition, it has an internal DC/DC voltage converter that generates various voltages needed for driving the TFT-LCD panel by using breeder resistance and the voltage follower.

2. Features

The key features of the IC are as follows:

- **384-ch (128-RGB) Source Driver & 160-ch Gate Driver**
- **Internal Graphic RAM (GRAM): 128 x 18 x 160 = 368,640 bits**
- **Support three different color display depths**
  262,144 colors can be displayed (including gamma adjust)
  65,536 colors, 8 colors can be displayed
- **CPU/RGB/SPI Interfaces**
  18-/16-/9-/8-bit high-speed parallel bus interfaces including MDT (Multiple Data Transfer) mode.
  3-/4-wire Serial Peripheral Interface (SPI)
  18-/16-/6-bit RGB interfaces for motion picture display
- **Enhancing functions for Graphic Operations**
  Window-Addressing Function to display motion picture independently of still image display
  Image Rotation & Mirroring Function
- **Toggling signal for TFT-LCD counter-electrode power (or AC VCOM)**
- **Low-power operation**
  Power-save functions (sleep mode, standby mode)
  Partial display (up to two separated screens) in any position
  Equalizing function for the switching performance of step-up circuits and operational amplifiers
- **Internal R-C oscillator and external hardware reset**
- **External power supply requirement**
  VDD3: 1.6 ~ 3.3V for I/O operation
  VCI : 2.5 ~ 3.3V for internal voltage-reference generation
- **Integrated DC/DC converters to provide several voltage supplies without Schottky diode.**
  DC/DC converter1 : V(AVDD, VSS) = 4.2 ~ 5.52V for the source driver array
  DC/DC converter2 : V(VGH, VGL) = 14.7 ~ 30.0V for the gate driver array
    - V(VGH, VSS) = 8.4 ~ 16.56V
    - V(VGL, VSS) = -13.8 ~ -6.3V
  DC/DC converter3 : V(VCL, VSS) = -2.76 ~ -2.1V for the TFT-LCD counter electrode.
- **Internally generated voltage sources**
  V(GVDD, VSS) = 3.0 ~ 5.0V for a reference power supply for grayscale voltages
  Vcom amplitude(max) = 6.0V for the TFT-LCD counter electrode
    - V(VcomH, VSS)max = GVDD
    - V(VomL, VSS)max =0 ~ (-VCI1 + 0.5V)

S6D0151 offers 2 ways to adjust VCOM amplitude. One way is by an external adjustment and the other by an internal adjustment, where the selection can be made via a register or MTP programming.

3. Display Module Block Diagram

3.1. Interface signal flow of the display module and its relationship

Figure 1 shows the block diagram of a mobile display panel module and related interface signals required by set makers and module makers. **Level I** interface signals represent the requirements of a set manufacturer that must be complied to by a module manufacturer. **Level II** interface signals, on the other hand, represent the requirements of the module manufacturer that, typically, a driver IC manufacturer must comply.

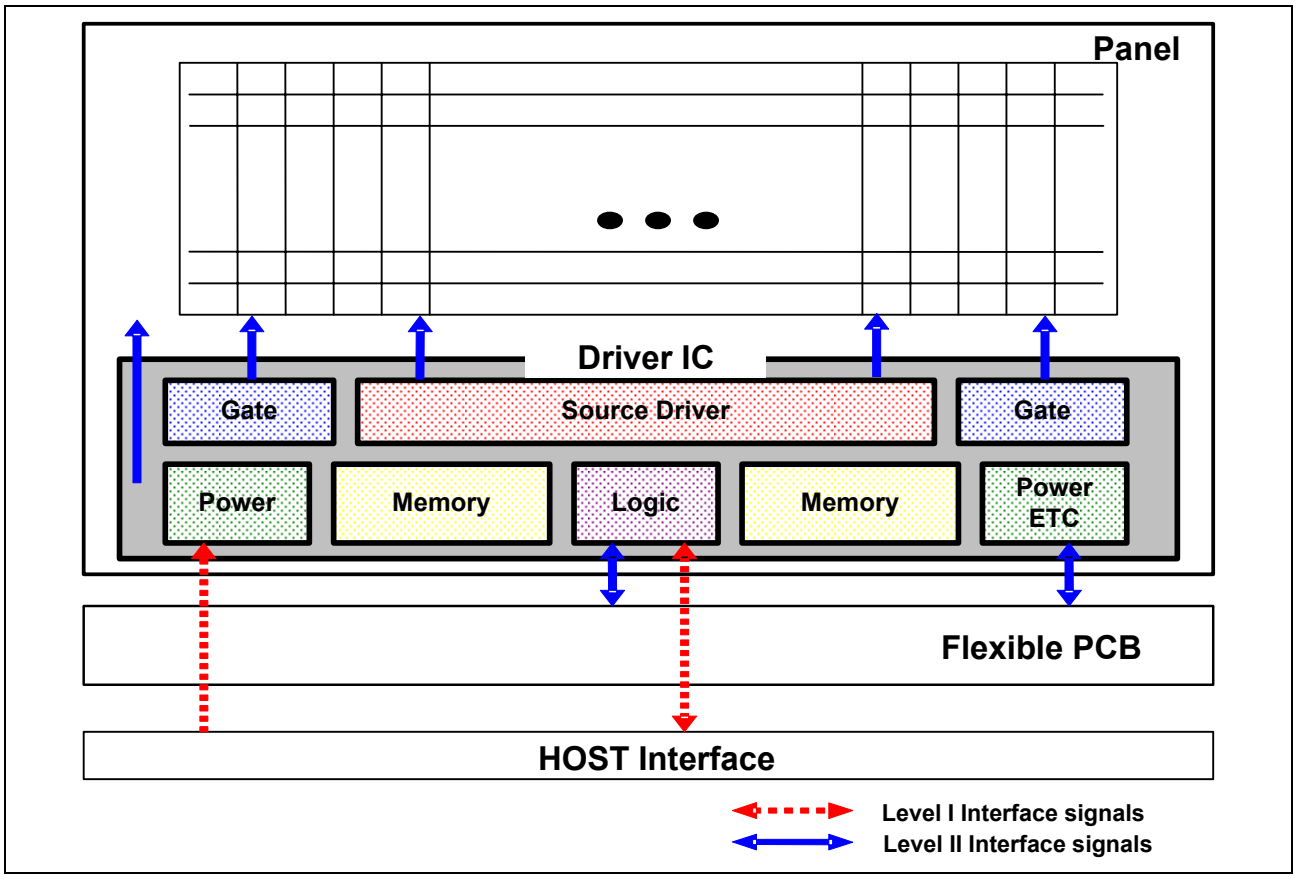


Figure 1. The interface signal flow of a mobile display panel module

There are also **Level III** signals which are for internal use only for the driver IC itself. These signals may not necessarily be released to the customer since they are designed for a specific manufacturing purpose and are supposed to be hidden from them.

The specifications shown in this document serve only as guidelines to Level I and II interface signals; the reason being that a specification related to Level I and II considers the parasitic and design requirements within the flexible PCB used by a display module maker. IC specification will offer related information among Level I/II on how each interface signals relates each other.

3.2. Functional block diagram

Figure 2 shows the overall functional block diagram of the IC. It consists of various functional blocks: Interface, timing control, source driver array, gate driver, power generation, oscillator, and other blocks.

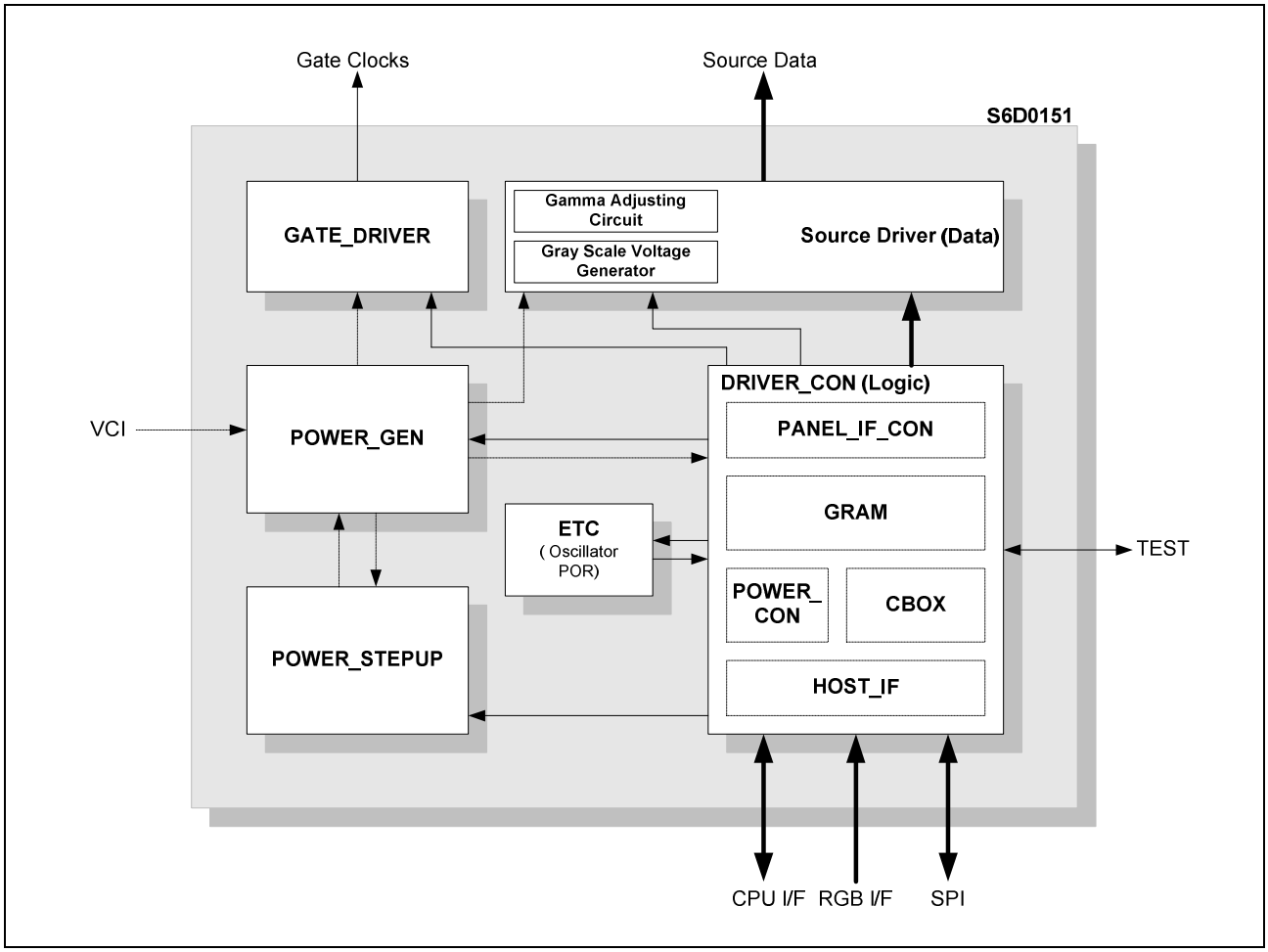


Figure 2. Functional block diagram of S6D0151.

4. Physical configuration of the Die

4.1. Pad configuration

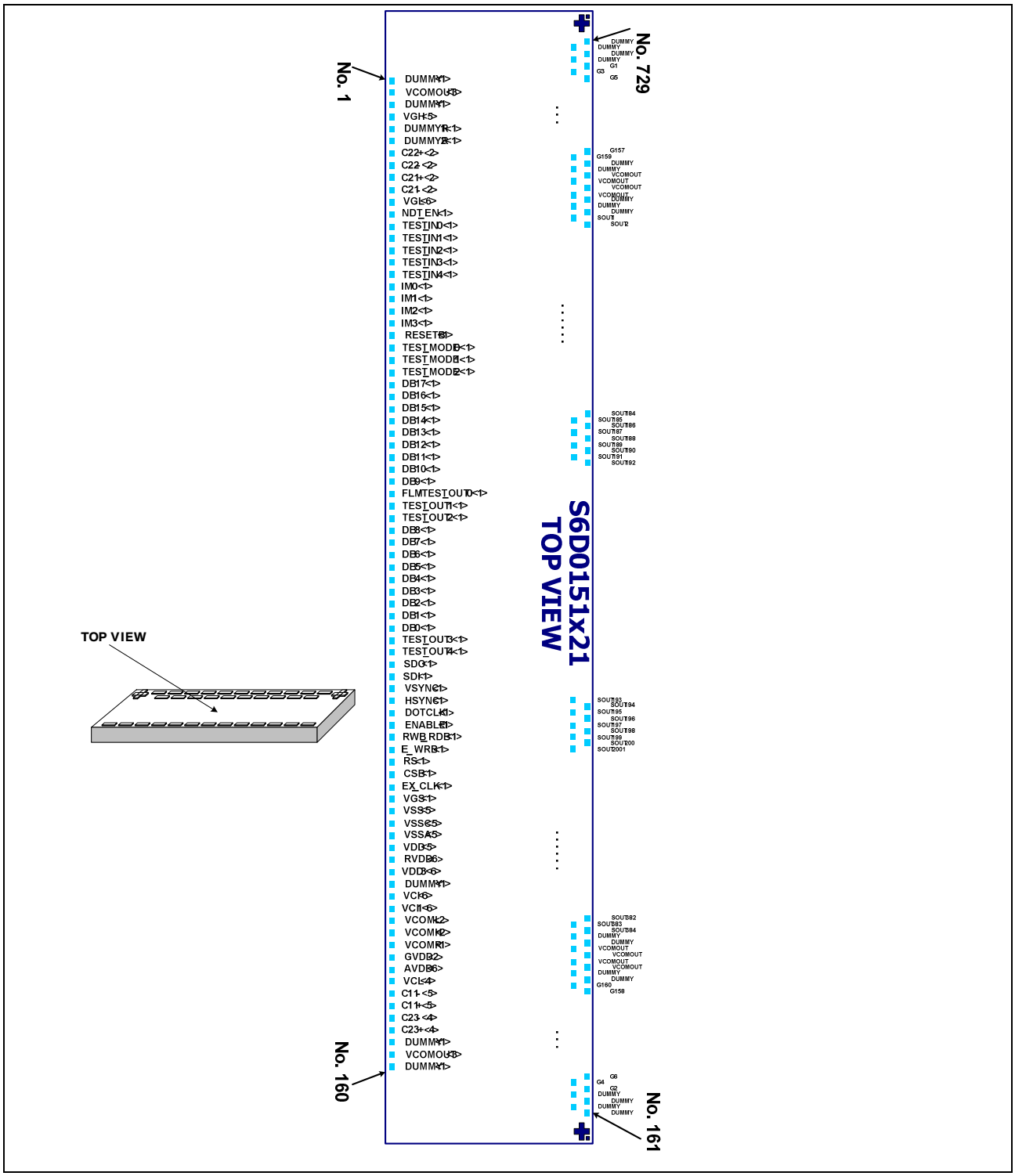


Figure 3. Configuration of pad layout.

Table 1. Physical dimensions of the IC

Items	Notation		Size	Unit
Die size[1)]	X (Length)		10560	μm
	Y (Width)		700	
	Thickness or height		Note 2	
Bump pad size	Input	E	76±2	
		F	40±2	
	Output	A	118±2	
		B	17±2	
Bump to bump	Output	D	35	
Bump pad pitch	Input	G	60 / 85	
	Output	C	16	
Bump pad height	on wafer	-	15(typ.) ±2	
	on die	-	< 1	

[Note]

1. Scribe lane included in this die size (Scribe lane width: 80 um)

2. Die thickness can be varies based on the customer's need.

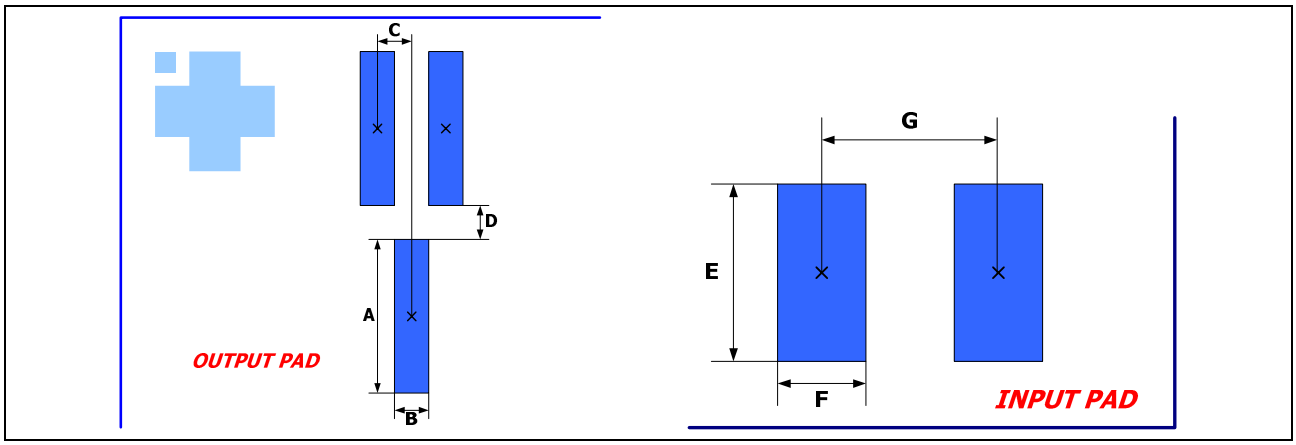


Figure 4. Input/output pad layout of the IC.

4.2. Align key configuration

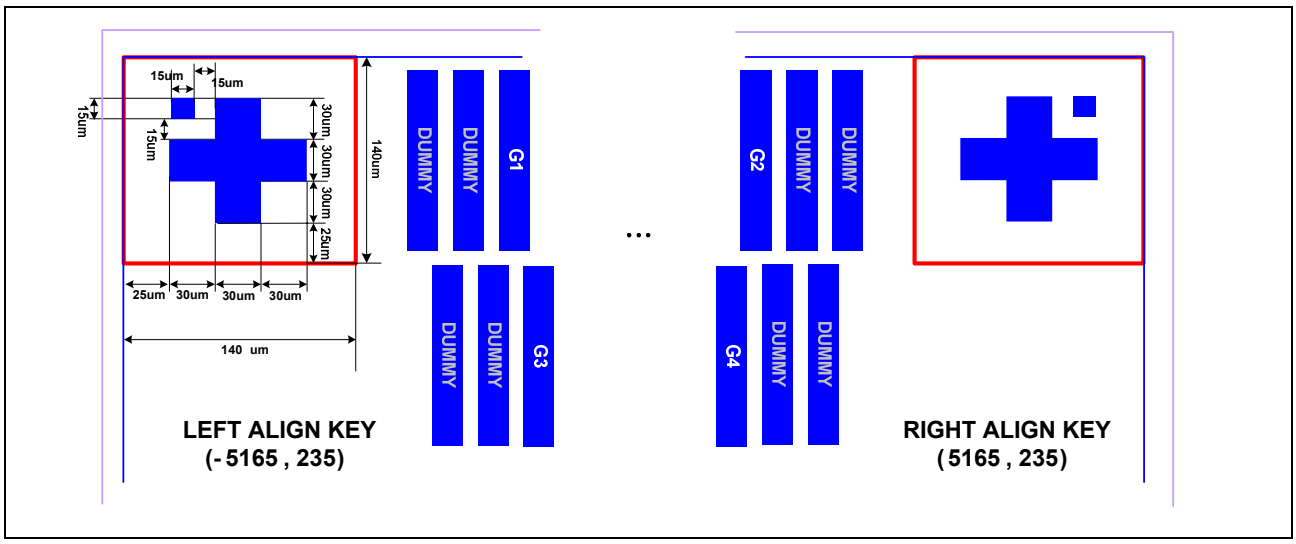


Figure 5. COG align key

4.3. Pad coordinates

Table 2. Coordinates at the center of each pad

[Unit : μm]

no.	X	Y	Pad Name
1	-5070	-265	DUMMY
2	-5010	-265	VCOMOUT
3	-4950	-265	VCOMOUT
4	-4890	-265	VCOMOUT
5	-4830	-265	DUMMY
6	-4770	-265	VGH
7	-4710	-265	VGH
8	-4650	-265	VGH
9	-4590	-265	VGH
10	-4530	-265	VGH
11	-4470	-265	DUMMYR1
12	-4410	-265	DUMMYR2
13	-4350	-265	C22+
14	-4290	-265	C22+
15	-4230	-265	C22-
16	-4170	-265	C22-
17	-4110	-265	C21+
18	-4050	-265	C21+
19	-3990	-265	C21-
20	-3930	-265	C21-
21	-3870	-265	VGL
22	-3810	-265	VGL
23	-3750	-265	VGL
24	-3690	-265	VGL
25	-3630	-265	VGL
26	-3570	-265	VGL
27	-3510	-265	NDT_EN
28	-3450	-265	TEST_IN0
29	-3390	-265	TEST_IN1
30	-3330	-265	TEST_IN2
31	-3270	-265	TEST_IN3
32	-3210	-265	TEST_IN4
33	-3150	-265	IM0
34	-3090	-265	IM1
35	-3030	-265	IM2
36	-2970	-265	IM3
37	-2910	-265	RESETB
38	-2850	-265	TEST_MODE1
39	-2790	-265	TEST_MODE2
40	-2730	-265	TEST_MODE3
41	-2670	-265	DB17
42	-2585	-265	DB16
43	-2500	-265	DB15
44	-2415	-265	DB14
45	-2330	-265	DB13
46	-2245	-265	DB12
47	-2160	-265	DB11
48	-2075	-265	DB10
49	-1990	-265	DB9
50	-1905	-265	FLM/TEST_OUT0
51	-1820	-265	TEST_OUT1
52	-1735	-265	TEST_OUT2
53	-1650	-265	DB8
54	-1565	-265	DB7
55	-1480	-265	DB6
56	-1395	-265	DB5
57	-1310	-265	DB4
58	-1225	-265	DB3
59	-1140	-265	DB2
60	-1055	-265	DB1
61	-970	-265	DB0
62	-885	-265	TEST_OUT3
63	-800	-265	TEST_OUT4
64	-715	-265	SDO
65	-630	-265	SDI
66	-570	-265	VSYNC
67	-510	-265	HSYNC
68	-450	-265	DOTCLK
69	-390	-265	ENABLE
70	-330	-265	RWB_RDB
71	-270	-265	E_WRB
72	-210	-265	RS
73	-150	-265	CSB
74	-90	-265	EX_CLK
75	-30	-265	VGS
76	30	-265	VSS
77	90	-265	VSS
78	150	-265	VSS
79	210	-265	VSS
80	270	-265	VSS
81	330	-265	VSSC
82	390	-265	VSSC
83	450	-265	VSSC
84	510	-265	VSSC
85	570	-265	VSSC
86	630	-265	VSSA
87	690	-265	VSSA
88	750	-265	VSSA
89	810	-265	VSSA
90	870	-265	VSSA
91	930	-265	VDD
92	990	-265	VDD
93	1050	-265	VDD
94	1110	-265	VDD
95	1170	-265	VDD
96	1230	-265	RVDD
97	1290	-265	RVDD
98	1350	-265	RVDD
99	1410	-265	RVDD
100	1470	-265	RVDD
101	1530	-265	RVDD
102	1590	-265	VDD3
103	1650	-265	VDD3
104	1710	-265	VDD3
105	1770	-265	VDD3
106	1830	-265	VDD3
107	1890	-265	VDD3
108	1950	-265	DUMMY
109	2010	-265	VCI
110	2070	-265	VCI
111	2130	-265	VCI
112	2190	-265	VCI
113	2250	-265	VCI
114	2310	-265	VCI
115	2370	-265	VCI1
116	2430	-265	VCI1
117	2490	-265	VCI1
118	2550	-265	VCI1
119	2610	-265	VCI1
120	2670	-265	VCI1
121	2730	-265	VCOML
122	2790	-265	VCOML
123	2850	-265	VCOMH
124	2910	-265	VCOMH
125	2970	-265	VCOMR
126	3030	-265	GVDD
127	3090	-265	GVDD
128	3150	-265	AVDD
129	3210	-265	AVDD
130	3270	-265	AVDD
131	3330	-265	AVDD
132	3390	-265	AVDD
133	3450	-265	AVDD
134	3510	-265	VCL
135	3570	-265	VCL
136	3630	-265	VCL
137	3690	-265	VCL
138	3750	-265	C11-
139	3810	-265	C11-
140	3870	-265	C11-
141	3930	-265	C11-
142	3990	-265	C11-
143	4050	-265	C11+
144	4110	-265	C11+
145	4170	-265	C11+
146	4230	-265	C11+
147	4290	-265	C11+
148	4350	-265	C23-
149	4410	-265	C23-
150	4470	-265	C23-

Table 3. Coordinates at the center of each pad

[Unit : μm]

no.	X	Y	Pad Name
151	4530	-265	C23-
152	4590	-265	C23+
153	4650	-265	C23+
154	4710	-265	C23+
155	4770	-265	C23+
156	4830	-265	DUMMY
157	4890	-265	VCOMOUT
158	4950	-265	VCOMOUT
159	5010	-265	VCOMOUT
160	5070	-265	DUMMY
161	5008	244	DUMMY
162	4992	91	DUMMY
163	4976	244	DUMMY
164	4960	91	DUMMY
165	4944	244	G2
166	4928	91	G4
167	4912	244	G6
168	4896	91	G8
169	4880	244	G10
170	4864	91	G12
171	4848	244	G14
172	4832	91	G16
173	4816	244	G18
174	4800	91	G20
175	4784	244	G22
176	4768	91	G24
177	4752	244	G26
178	4736	91	G28
179	4720	244	G30
180	4704	91	G32
181	4688	244	G34
182	4672	91	G36
183	4656	244	G38
184	4640	91	G40
185	4624	244	G42
186	4608	91	G44
187	4592	244	G46
188	4576	91	G48
189	4560	244	G50
190	4544	91	G52
191	4528	244	G54
192	4512	91	G56
193	4496	244	G58
194	4480	91	G60
195	4464	244	G62
196	4448	91	G64
197	4432	244	G66
198	4416	91	G68
199	4400	244	G70
200	4384	91	G72
201	4368	244	G74
202	4352	91	G76
203	4336	244	G78
204	4320	91	G80
205	4304	244	G82
206	4288	91	G84
207	4272	244	G86
208	4256	91	G88
209	4240	244	G90
210	4224	91	G92
211	4208	244	G94
212	4192	91	G96
213	4176	244	G98
214	4160	91	G100
215	4144	244	G102
216	4128	91	G104
217	4112	244	G106
218	4096	91	G108
219	4080	244	G110
220	4064	91	G112
221	4048	244	G114
222	4032	91	G116
223	4016	244	G118
224	4000	91	G120
225	3984	244	G122
226	3968	91	G124
227	3952	244	G126
228	3936	91	G128
229	3920	244	G130
230	3904	91	G132
231	3888	244	G134
232	3872	91	G136
233	3856	244	G138
234	3840	91	G140
235	3824	244	G142
236	3808	91	G144
237	3792	244	G146
238	3776	91	G148
239	3760	244	G150
240	3744	91	G152
241	3728	244	G154
242	3712	91	G156
243	3696	244	G158
244	3680	91	G160
245	3664	244	DUMMY
246	3648	91	DUMMY
247	3632	244	VCOMOUT
248	3616	91	VCOMOUT
249	3600	244	VCOMOUT
250	3584	91	VCOMOUT
251	3568	244	DUMMY
252	3552	91	DUMMY
253	3536	244	SOUT384
254	3520	91	SOUT383
255	3504	244	SOUT382
256	3488	91	SOUT381
257	3472	244	SOUT380
258	3456	91	SOUT379
259	3440	244	SOUT378
260	3424	91	SOUT377
261	3408	244	SOUT376
262	3392	91	SOUT375
263	3376	244	SOUT374
264	3360	91	SOUT373
265	3344	244	SOUT372
266	3328	91	SOUT371
267	3312	244	SOUT370
268	3296	91	SOUT369
269	3280	244	SOUT368
270	3264	91	SOUT367
271	3248	244	SOUT366
272	3232	91	SOUT365
273	3216	244	SOUT364
274	3200	91	SOUT363
275	3184	244	SOUT362
276	3168	91	SOUT361
277	3152	244	SOUT360
278	3136	91	SOUT359
279	3120	244	SOUT358
280	3104	91	SOUT357
281	3088	244	SOUT356
282	3072	91	SOUT355
283	3056	244	SOUT354
284	3040	91	SOUT353
285	3024	244	SOUT352
286	3008	91	SOUT351
287	2992	244	SOUT350
288	2976	91	SOUT349
289	2960	244	SOUT348
290	2944	91	SOUT347
291	2928	244	SOUT346
292	2912	91	SOUT345
293	2896	244	SOUT344
294	2880	91	SOUT343
295	2864	244	SOUT342
296	2848	91	SOUT341
297	2832	244	SOUT340
298	2816	91	SOUT339
299	2800	244	SOUT338
300	2784	91	SOUT337

Table 4. Coordinates at the center of each pad

[Unit : μm]

no.	X	Y	Pad Name
301	2768	244	SOUT336
302	2752	91	SOUT335
303	2736	244	SOUT334
304	2720	91	SOUT333
305	2704	244	SOUT332
306	2688	91	SOUT331
307	2672	244	SOUT330
308	2656	91	SOUT329
309	2640	244	SOUT328
310	2624	91	SOUT327
311	2608	244	SOUT326
312	2592	91	SOUT325
313	2576	244	SOUT324
314	2560	91	SOUT323
315	2544	244	SOUT322
316	2528	91	SOUT321
317	2512	244	SOUT320
318	2496	91	SOUT319
319	2480	244	SOUT318
320	2464	91	SOUT317
321	2448	244	SOUT316
322	2432	91	SOUT315
323	2416	244	SOUT314
324	2400	91	SOUT313
325	2384	244	SOUT312
326	2368	91	SOUT311
327	2352	244	SOUT310
328	2336	91	SOUT309
329	2320	244	SOUT308
330	2304	91	SOUT307
331	2288	244	SOUT306
332	2272	91	SOUT305
333	2256	244	SOUT304
334	2240	91	SOUT303
335	2224	244	SOUT302
336	2208	91	SOUT301
337	2192	244	SOUT300
338	2176	91	SOUT299
339	2160	244	SOUT298
340	2144	91	SOUT297
341	2128	244	SOUT296
342	2112	91	SOUT295
343	2096	244	SOUT294
344	2080	91	SOUT293
345	2064	244	SOUT292
346	2048	91	SOUT291
347	2032	244	SOUT290
348	2016	91	SOUT289
349	2000	244	SOUT288
350	1984	91	SOUT287
351	1968	244	SOUT286
352	1952	91	SOUT285
353	1936	244	SOUT284
354	1920	91	SOUT283
355	1904	244	SOUT282
356	1888	91	SOUT281
357	1872	244	SOUT280
358	1856	91	SOUT279
359	1840	244	SOUT278
360	1824	91	SOUT277
361	1808	244	SOUT276
362	1792	91	SOUT275
363	1776	244	SOUT274
364	1760	91	SOUT273
365	1744	244	SOUT272
366	1728	91	SOUT271
367	1712	244	SOUT270
368	1696	91	SOUT269
369	1680	244	SOUT268
370	1664	91	SOUT267
371	1648	244	SOUT266
372	1632	91	SOUT265
373	1616	244	SOUT264
374	1600	91	SOUT263
375	1584	244	SOUT262
376	1568	91	SOUT261
377	1552	244	SOUT260
378	1536	91	SOUT259
379	1520	244	SOUT258
380	1504	91	SOUT257
381	1488	244	SOUT256
382	1472	91	SOUT255
383	1456	244	SOUT254
384	1440	91	SOUT253
385	1424	244	SOUT252
386	1408	91	SOUT251
387	1392	244	SOUT250
388	1376	91	SOUT249
389	1360	244	SOUT248
390	1344	91	SOUT247
391	1328	244	SOUT246
392	1312	91	SOUT245
393	1296	244	SOUT244
394	1280	91	SOUT243
395	1264	244	SOUT242
396	1248	91	SOUT241
397	1232	244	SOUT240
398	1216	91	SOUT239
399	1200	244	SOUT238
400	1184	91	SOUT237
401	1168	244	SOUT236
402	1152	91	SOUT235
403	1136	244	SOUT234
404	1120	91	SOUT233
405	1104	244	SOUT232
406	1088	91	SOUT231
407	1072	244	SOUT230
408	1056	91	SOUT229
409	1040	244	SOUT228
410	1024	91	SOUT227
411	1008	244	SOUT226
412	992	91	SOUT225
413	976	244	SOUT224
414	960	91	SOUT223
415	944	244	SOUT222
416	928	91	SOUT221
417	912	244	SOUT220
418	896	91	SOUT219
419	880	244	SOUT218
420	864	91	SOUT217
421	848	244	SOUT216
422	832	91	SOUT215
423	816	244	SOUT214
424	800	91	SOUT213
425	784	244	SOUT212
426	768	91	SOUT211
427	752	244	SOUT210
428	736	91	SOUT209
429	720	244	SOUT208
430	704	91	SOUT207
431	688	244	SOUT206
432	672	91	SOUT205
433	656	244	SOUT204
434	640	91	SOUT203
435	624	244	SOUT202
436	608	91	SOUT201
437	592	244	SOUT200
438	576	91	SOUT199
439	560	244	SOUT198
440	544	91	SOUT197
441	528	244	SOUT196
442	512	91	SOUT195
443	496	244	SOUT194
444	480	91	SOUT193
445	-466	244	SOUT192
446	-482	91	SOUT191
447	-498	244	SOUT190
448	-514	91	SOUT189
449	-530	244	SOUT188
450	-546	91	SOUT187

Table 5. Coordinates at the center of each pad

[Unit : μm]

no.	X	Y	Pad Name
451	-562	244	SOUT186
452	-578	91	SOUT185
453	-594	244	SOUT184
454	-610	91	SOUT183
455	-626	244	SOUT182
456	-642	91	SOUT181
457	-658	244	SOUT180
458	-674	91	SOUT179
459	-690	244	SOUT178
460	-706	91	SOUT177
461	-722	244	SOUT176
462	-738	91	SOUT175
463	-754	244	SOUT174
464	-770	91	SOUT173
465	-786	244	SOUT172
466	-802	91	SOUT171
467	-818	244	SOUT170
468	-834	91	SOUT169
469	-850	244	SOUT168
470	-866	91	SOUT167
471	-882	244	SOUT166
472	-898	91	SOUT165
473	-914	244	SOUT164
474	-930	91	SOUT163
475	-946	244	SOUT162
476	-962	91	SOUT161
477	-978	244	SOUT160
478	-994	91	SOUT159
479	-1010	244	SOUT158
480	-1026	91	SOUT157
481	-1042	244	SOUT156
482	-1058	91	SOUT155
483	-1074	244	SOUT154
484	-1090	91	SOUT153
485	-1106	244	SOUT152
486	-1122	91	SOUT151
487	-1138	244	SOUT150
488	-1154	91	SOUT149
489	-1170	244	SOUT148
490	-1186	91	SOUT147
491	-1202	244	SOUT146
492	-1218	91	SOUT145
493	-1234	244	SOUT144
494	-1250	91	SOUT143
495	-1266	244	SOUT142
496	-1282	91	SOUT141
497	-1298	244	SOUT140
498	-1314	91	SOUT139
499	-1330	244	SOUT138
500	-1346	91	SOUT137
501	-1362	244	SOUT136
502	-1378	91	SOUT135
503	-1394	244	SOUT134
504	-1410	91	SOUT133
505	-1426	244	SOUT132
506	-1442	91	SOUT131
507	-1458	244	SOUT130
508	-1474	91	SOUT129
509	-1490	244	SOUT128
510	-1506	91	SOUT127
511	-1522	244	SOUT126
512	-1538	91	SOUT125
513	-1554	244	SOUT124
514	-1570	91	SOUT123
515	-1586	244	SOUT122
516	-1602	91	SOUT121
517	-1618	244	SOUT120
518	-1634	91	SOUT119
519	-1650	244	SOUT118
520	-1666	91	SOUT117
521	-1682	244	SOUT116
522	-1698	91	SOUT115
523	-1714	244	SOUT114
524	-1730	91	SOUT113
525	-1746	244	SOUT112
526	-1762	91	SOUT111
527	-1778	244	SOUT110
528	-1794	91	SOUT109
529	-1810	244	SOUT108
530	-1826	91	SOUT107
531	-1842	244	SOUT106
532	-1858	91	SOUT105
533	-1874	244	SOUT104
534	-1890	91	SOUT103
535	-1906	244	SOUT102
536	-1922	91	SOUT101
537	-1938	244	SOUT100
538	-1954	91	SOUT99
539	-1970	244	SOUT98
540	-1986	91	SOUT97
541	-2002	244	SOUT96
542	-2018	91	SOUT95
543	-2034	244	SOUT94
544	-2050	91	SOUT93
545	-2066	244	SOUT92
546	-2082	91	SOUT91
547	-2098	244	SOUT90
548	-2114	91	SOUT89
549	-2130	244	SOUT88
550	-2146	91	SOUT87
551	-2162	244	SOUT86
552	-2178	91	SOUT85
553	-2194	244	SOUT84
554	-2210	91	SOUT83
555	-2226	244	SOUT82
556	-2242	91	SOUT81
557	-2258	244	SOUT80
558	-2274	91	SOUT79
559	-2290	244	SOUT78
560	-2306	91	SOUT77
561	-2322	244	SOUT76
562	-2338	91	SOUT75
563	-2354	244	SOUT74
564	-2370	91	SOUT73
565	-2386	244	SOUT72
566	-2402	91	SOUT71
567	-2418	244	SOUT70
568	-2434	91	SOUT69
569	-2450	244	SOUT68
570	-2466	91	SOUT67
571	-2482	244	SOUT66
572	-2498	91	SOUT65
573	-2514	244	SOUT64
574	-2530	91	SOUT63
575	-2546	244	SOUT62
576	-2562	91	SOUT61
577	-2578	244	SOUT60
578	-2594	91	SOUT59
579	-2610	244	SOUT58
580	-2626	91	SOUT57
581	-2642	244	SOUT56
582	-2658	91	SOUT55
583	-2674	244	SOUT54
584	-2690	91	SOUT53
585	-2706	244	SOUT52
586	-2722	91	SOUT51
587	-2738	244	SOUT50
588	-2754	91	SOUT49
589	-2770	244	SOUT48
590	-2786	91	SOUT47
591	-2802	244	SOUT46
592	-2818	91	SOUT45
593	-2834	244	SOUT44
594	-2850	91	SOUT43
595	-2866	244	SOUT42
596	-2882	91	SOUT41
597	-2898	244	SOUT40
598	-2914	91	SOUT39
599	-2930	244	SOUT38
600	-2946	91	SOUT37

Table 6. Coordinates at the center of each pad

[Unit : μm]

no.	X	Y	Pad Name
601	-2962	244	SOUT36
602	-2978	91	SOUT35
603	-2994	244	SOUT34
604	-3010	91	SOUT33
605	-3026	244	SOUT32
606	-3042	91	SOUT31
607	-3058	244	SOUT30
608	-3074	91	SOUT29
609	-3090	244	SOUT28
610	-3106	91	SOUT27
611	-3122	244	SOUT26
612	-3138	91	SOUT25
613	-3154	244	SOUT24
614	-3170	91	SOUT23
615	-3186	244	SOUT22
616	-3202	91	SOUT21
617	-3218	244	SOUT20
618	-3234	91	SOUT19
619	-3250	244	SOUT18
620	-3266	91	SOUT17
621	-3282	244	SOUT16
622	-3298	91	SOUT15
623	-3314	244	SOUT14
624	-3330	91	SOUT13
625	-3346	244	SOUT12
626	-3362	91	SOUT11
627	-3378	244	SOUT10
628	-3394	91	SOUT9
629	-3410	244	SOUT8
630	-3426	91	SOUT7
631	-3442	244	SOUT6
632	-3458	91	SOUT5
633	-3474	244	SOUT4
634	-3490	91	SOUT3
635	-3506	244	SOUT2
636	-3522	91	SOUT1
637	-3538	244	DUMMY
638	-3554	91	DUMMY
639	-3570	244	DUMMY
640	-3586	91	VCOMOUT
641	-3602	244	VCOMOUT
642	-3618	91	VCOMOUT
643	-3634	244	VCOMOUT
644	-3650	91	DUMMY
645	-3666	244	DUMMY
646	-3682	91	G159
647	-3698	244	G157
648	-3714	91	G155
649	-3730	244	G153
650	-3746	91	G151
651	-3762	244	G149
652	-3778	91	G147
653	-3794	244	G145
654	-3810	91	G143
655	-3826	244	G141
656	-3842	91	G139
657	-3858	244	G137
658	-3874	91	G135
659	-3890	244	G133
660	-3906	91	G131
661	-3922	244	G129
662	-3938	91	G127
663	-3954	244	G125
664	-3970	91	G123
665	-3986	244	G121
666	-4002	91	G119
667	-4018	244	G117
668	-4034	91	G115
669	-4050	244	G113
670	-4066	91	G111
671	-4082	244	G109
672	-4098	91	G107
673	-4114	244	G105
674	-4130	91	G103
675	-4146	244	G101
676	-4162	91	G99
677	-4178	244	G97
678	-4194	91	G95
679	-4210	244	G93
680	-4226	91	G91
681	-4242	244	G89
682	-4258	91	G87
683	-4274	244	G85
684	-4290	91	G83
685	-4306	244	G81
686	-4322	91	G79
687	-4338	244	G77
688	-4354	91	G75
689	-4370	244	G73
690	-4386	91	G71
691	-4402	244	G69
692	-4418	91	G67
693	-4434	244	G65
694	-4450	91	G63
695	-4466	244	G61
696	-4482	91	G59
697	-4498	244	G57
698	-4514	91	G55
699	-4530	244	G53
700	-4546	91	G51
701	-4562	244	G49
702	-4578	91	G47
703	-4594	244	G45
704	-4610	91	G43
705	-4626	244	G41
706	-4642	91	G39
707	-4658	244	G37
708	-4674	91	G35
709	-4690	244	G33
710	-4706	91	G31
711	-4722	244	G29
712	-4738	91	G27
713	-4754	244	G25
714	-4770	91	G23
715	-4786	244	G21
716	-4802	91	G19
717	-4818	244	G17
718	-4834	91	G15
719	-4850	244	G13
720	-4866	91	G11
721	-4882	244	G9
722	-4898	91	G7
723	-4914	244	G5
724	-4930	91	G3
725	-4946	244	G1
726	-4962	91	DUMMY
727	-4978	244	DUMMY
728	-4994	91	DUMMY
729	-5010	244	DUMMY

5. Description of the Signal Pads

Table 7. Pad description for Power supplies

Name	I/O	Level	Description
VDD3	Power	I	Power supply (1.6 ~ 3.3V) to the I/O block of the IC.
VCI	Power	I	Power supply (2.5 ~ 3.3V) to the internal reference circuits. Use the same power supply as VDD3 if VDD3 = 2.5 ~ 3.3V. Otherwise, use a power supply which covers 2.5 ~ 3.3V.
VDD	Power	III	Internally generated power supply to various internal blocks. Must be tied to RVDD pad.
RVDD	Power Output	III	This voltage source is regulated from VCI and used as power supply to the internal logic circuits. Connect an external capacitor for stabilization.
AVDD	Power	II	An external capacitor should be connected between AVDD and a ground reference. This voltage is internally generated from VCI1 and used for supplying a power to the source driver array. AVDD ranges from 3.5 ~ 5.5V.
GVDD	Power	II	An external capacitor should be connected between GVDD and a ground reference for stabilization. This voltage source is an upper-end reference for the grayscale voltage generator.
VSS	Power	I	Ground reference (0V)
VSSC	Power	II	Ground reference for the DC/DC converter circuitry.
VSSA	Power	II	Ground reference for analog circuit blocks.
VGS	Power	II	Reference voltage source for the gamma reference voltage generator.
VCI1	Power	III	An external capacitor should be connected between VCI1 and a ground reference for stabilization. This voltage source is regulated from VCI and used as a reference voltage for the AVDD generation.
VCL	Power	II	An external capacitor should be connected between VCL and a ground reference for stabilization. This source is used as the power supply for generating VcomL.
VcomOUT	Power, Output	II	This is internally generated signal and needs to be connected to the TFT-display counter electrode. This pad is also used as equalizing function: During EQ = High period, all outputs of the source driver array are connected to VcomOUT level (Hi-z).
VcomR	Power, Input	II	A reference level for VcomH & VcomL. When VcomH is adjusted by an external source, the internal adjuster of VcomH should be disabled by setting the specific register and a variable resistor between GVDD and VSS be placed. When this pad is not externally adjusted, leave it unconnected and adjust VcomH by setting the internal register.
VcomH	Power, Output	II	An external capacitor should be connected between VcomH and a ground reference for stabilization. This signal outputs the high level of VCOM voltage signal as it toggles.
VcomL	Power, Output	III	This signal outputs the low level of Vcom voltage signal as it toggles. An internal register can be used to adjust the voltage. Connect this pad to an external capacitor for stabilization. When VCOMG bit is set to logic low, VcomL output stops and a capacitor for stabilization would not be needed.

Table 8. Pad description for power supplies (continued)

Pad Name	I/O	Level	Description
VGH	Power, Output	II	A positive power output pad for the gate driver, internal voltage step-up circuits, bias circuits, and operational amplifiers. Connect a capacitor for stabilization.
VGL	Power, Output	II	A negative power output pad for the gate driver, bias circuits, and operational amplifiers. To protect IC against latch up, connect the cathode of the schottky diode to the VSS pad. And the anode of the schottky diode to the VGL pad. Refer to application circuit. For using S6D0151 without external Schottky diode, additional registers should be set following Set-up Flow of DC/DC Converter without Schottky Diode. Refer to Timing Diagram of Power Setting section. This pad should be connected to an external capacitor for stabilization.
C11+/C11-	-	II	For external capacitor connection which is used for generating the AVDD level.
C22+/C22- C21+/C21-	-	II	For external capacitor connection which is used for generating the VGL/VGH level.
C23+/C23-	-	II	For external capacitor connection which is used for generating the VCL level.

Table 9. Pad description for CPU interface.

<table>
<tr><th>Pad Name</th><th>I/O</th><th>Level</th><th>Description</th></tr>
<tr><td>IM[3:0] / ID</td><td>I</td><td>I</td><td>Selects the System interface mode.
<table>
<tr><th>IM[3:0]</th><th>Description</th></tr>
<tr><td>4’b0000</td><td>68-Series 16-bit CPU interface</td></tr>
<tr><td>4’b0001</td><td>68-Series 8-bit CPU interface</td></tr>
<tr><td>4’b0010</td><td>80-Series 16-bit CPU interface</td></tr>
<tr><td>4’b0011</td><td>80-Series 8-bit CPU interface</td></tr>
<tr><td>4’b010x</td><td>4-wire Serial peripheral interface (4-wire SPI)
IM[0] = ID</td></tr>
<tr><td>4’b0110</td><td>Reserved</td></tr>
<tr><td>4’b0111</td><td>3-wire Serial peripheral interface (3-wire SPI)
IM[0] = ID = 1’b1</td></tr>
<tr><td>4’b1000</td><td>68-Series 18-bit CPU interface</td></tr>
<tr><td>4’b1001</td><td>68-Series 9-bit CPU interface</td></tr>
<tr><td>4’b1010</td><td>80-Series 18-bit CPU interface</td></tr>
<tr><td>4’b1011</td><td>80-Series 9-bit CPU interface</td></tr>
<tr><td>4’b11xx</td><td>Reserved</td></tr>
</table></td></tr>
<tr><td>CSB</td><td>I</td><td>I</td><td>Chip select:
- Low: S6D0151 is selected and can be accessed.
- High: S6D0151 is not selected and cannot be accessed.
Must be tied to VDD3 level when not in use.</td></tr>
<tr><td>RS</td><td>I</td><td>I</td><td>Register select.
- Low : select Index / status register
- High : select Control register
In 3-wire SPI mode, it serves as a synchronous clock
Must be tied to VDD3 or VSS level when 4-wire SPI mode.</td></tr>
<tr><td>E_WRB / SCL</td><td>I</td><td>I</td><td>In 68-Series mode, this serves as write/read enable strobe (E).
In 80-Series mode, this serves as a write strobe signal (WRB).
In 4-wire SPI mode, it serves as a synchronous clock (SCL).
Must be tied to VDD3 or VSS level when 3-wire SPI mode.</td></tr>
<tr><td>RWB_RDB</td><td>I</td><td>I</td><td>In 68-Series mode, this is used to select Read/Write (RWB) operation
In 80-Series mode, this serves as a Read Strobe Signal. (RDB).
Must be tied to VDD3 or VSS level when SPI mode.</td></tr>
<tr><td>DB[17:0]
[NOTE]</td><td>I/O</td><td>I</td><td>Data Bus.
<table>
<tr><th>IM[3:0]</th><th>Interface Mode</th><th>Index</th><th>Data</th></tr>
<tr><td>4’b0000</td><td>68-Series 16-bit CPU interface</td><td>DB[8:1]</td><td>DB[17:10], DB[8:1]</td></tr>
<tr><td>4’b0001</td><td>68-Series 8-bit CPU interface</td><td>DB[17:10]</td><td>DB[17:10]</td></tr>
<tr><td>4’b0010</td><td>80-Series 16-bit CPU interface</td><td>DB[8:1]</td><td>DB[17:10], DB[8:1]</td></tr>
<tr><td>4’b0011</td><td>80-Series 8-bit CPU interface</td><td>DB[17:10]</td><td>DB[17:10]</td></tr>
<tr><td>4’b010x</td><td>4-wire Serial peripheral interface (4-wire SPI)</td><td>-</td><td>-</td></tr>
<tr><td>4’b0110</td><td>Reserved</td><td>-</td><td>-</td></tr>
<tr><td>4’b0111</td><td>3-wire Serial peripheral interface (3-wire SPI)</td><td>DB[10]</td><td>DB[10]</td></tr>
<tr><td>4’b1000</td><td>68-Series 18-bit CPU interface</td><td>DB[8:1]</td><td>DB[17:0]</td></tr>
<tr><td>4’b1001</td><td>68-Series 9-bit CPU interface</td><td>DB[17:10]</td><td>DB[17:9]</td></tr>
<tr><td>4’b1010</td><td>80-Series 18-bit CPU interface</td><td>DB[8:1]</td><td>DB[17:0]</td></tr>
<tr><td>4’b1011</td><td>80-Series 9-bit CPU interface</td><td>DB[17:10]</td><td>DB[17:9]</td></tr>
<tr><td>4’b11xx</td><td>Reserved</td><td>-</td><td>-</td></tr>
</table>
Must be tied to VDD3 or VSS level when not used.</td></tr>
<tr><td>SDI</td><td>I</td><td>I</td><td>4-wire SPI Mode Serial input data. Must be tied to VDD3 or VSS level when not in use.</td></tr>
<tr><td>SDO</td><td>O</td><td></td><td>4-wire SPI Mode Serial output data. Leave this pad unconnected when not in use.</td></tr>
</table>

[Note] When used as system interface.

Table 10. Pad description for RGB interface.

Pad Name	I/O	Level	Description
ENABLE	I	I	Data enable signal for the RGB interface. When ENABLE is in active state, data on DB[17:0] is valid, but when this is not in active state, data on DB[17:0] is invalid. (For details, refer to the description of EPL register) Must be tied to VDD3 level when not in use.
VSYNC	I	I	Synchronous signal for a frame. (active low) Must be tied to VDD3 or VSS level when not in use.
HSYNC	I	I	Synchronization signal for a horizontal line. (active low) Must be tied to VDD3 or VSS level when not in use.
DOTCLK	I	I	Data Clock of RGB interface. Must be tied to VDD3 or VSS level when not in use.
DB[17:0] [NOTE]	I	I	Serves as an input data bus for RGB I/F. - 6-bit interface: DB[17:12] - 16-bit interface: {DB[17:13], DB[11:1]} - 18-bit interface: DB[17:0] Must be tied to VDD3 or VSS level when not in use.

[Note] When used as RGB I/F

Table 11. Pad description for display.

Pad Name	I/O	Level	Description
S1 ~ S384	O	II	Source driver output pads. The SS bit can change the shift direction of the source signal. For example, if SS = 0, the pixel data of S1 is read from RAM address 0000h. If SS = 1, the pixel data of S384 is read from RAM address 0000h. S1, S4, S7, ... S(3n-1) : display Red (R) (SS = 0) S2, S5, S8, ... S(3n-2) : display Green (G) (SS = 0) S3, S6, S9, ... S(3n) : display Blue (B) (SS = 0)
G1 ~ G160	O	II	Gate driver output pads. The output of gate driver is either VGH or VGL VGH : gate-ON level VGL : gate-OFF level

Table 12. Pad description for Reset.

Symbol	I/O	Level	Description
RESETB	I	I	Reset pad. Initializes the IC when low. Must be reset after power-on. Leave this pad open when not used. Refer to the RESESTB Signal section.

Table 13. Other pads.

<table>
<tr><th>Symbol</th><th>I/O</th><th>Level</th><th>Description</th></tr>
<tr><td>TEST_IN[2:0]</td><td>I</td><td>III</td><td>Test pad. During the normal operation, either leave this pad unconnected or tied to ground.</td></tr>
<tr><td>TEST_IN[4:3]</td><td>I</td><td>I</td><td>The value of RB6h depends on the external connections to TEST_IN[4:3] pads.
<table>
<tr><th>TEST_IN[4]</th><th>TEST_IN[3]</th><th>Read-out value of RB6h</th></tr>
<tr><td>tie to VSS</td><td>tie to VSS</td><td>013fh</td></tr>
<tr><td>tie to VSS</td><td>tie to VDD3</td><td>413fh</td></tr>
<tr><td>tie to VDD3</td><td>tie to VSS</td><td>813fh</td></tr>
<tr><td>tie to VDD3</td><td>tie to VDD3</td><td>c13fh</td></tr>
<tr><td>Floating</td><td>Floating</td><td>013fh</td></tr>
</table></td></tr>
<tr><td>TEST_MODE [2:0]</td><td>I</td><td>III</td><td>Test pad. During the normal operation, either leave this pad unconnected or tied to ground.</td></tr>
<tr><td>FLM/ TEST_OUT[0]</td><td>O</td><td>III</td><td>Frame start signal. Leave this pad unconnected when not in use.</td></tr>
<tr><td>TEST_OUT [4:1]</td><td>O</td><td>III</td><td>Test pad. During the normal operation, leave this pad unconnected.</td></tr>
<tr><td>DUMMY</td><td>-</td><td>III</td><td>Dummy pad. These pads have no connection to the internal circuitry.</td></tr>
<tr><td>EX_CLK</td><td>I</td><td>III</td><td>Test pad. During the normal operation, either leave this pad unconnected or tied to VDD3.</td></tr>
<tr><td>NDT_EN</td><td>I</td><td>III</td><td>Test signal input pad. During the normal operation, either leave this pad unconnected or tied to VSS level.</td></tr>
<tr><td>DUMMYR1, DUMMYR2</td><td>-</td><td>II</td><td>Pads for conducting contact resistance measurements. During the normal operation, leave this pad unconnected</td></tr>
</table>

6. Electrical Specifications

6.1. Absolute maximum ratings

Table 14. Absolute Maximum Ratings

(VSS = 0V).

Function	Symbol	Rating	Unit
Supply voltage (VDD3) to I/O block	VDD3 *1	-0.3 ~ 5.5	V
Supply voltage (VCI) to the voltage step-up circuit	VCI *1	-0.3 ~ 5.5	
LCD Supply Voltage range: AVDD, VGH, VGL, & VCL	AVDD *1	-0.3 ~ 6.5	
	VGH *1	-0.3 ~ 22.0	
	|VSS – VGL|	-0.3 ~ 22.0	
	VSS - VCL	-0.3 ~ 5.0	
	|VGH – VGL|	-0.3 ~ 33	
Input Voltage range	Vin	- 0.3 ~ VDD3 +0.5	
Operating temperature	T_{op}	-40 ~ +85	°C
Storage temperature	$T_{storage}$	-55 ~ +110	°C

[Note] *1) Against VSS.

Caution

Stresses above these absolute maximum ratings may cause permanent damage. These are stress ratings only and functional operation at these conditions is not implied. Exposure to maximum rating conditions for extended periods may reduce device reliability

6.2. DC electrical characteristics

Table 15. DC Characteristics

(Condition: VSS = 0V, T_{OP} = -40°C ~ 85°C)

Parameters	Symbol	Condition	Min.	Typ.	Max.	Unit	Note
Power supply to the I/O	VDD3		1.6		3.3	V	
Power supply to the Internal reference	VCI		2.5	-	3.3	V	
LCD driving voltage (internally generated)	VGH	Without Load	8.4		16.56	V	
	VGL	Without Load	-13.8		-6.3	V	
	AVDD	Without Load	4.1		5.52	V	
Input voltage, high	V_{IH}		0.8*VDD3		VDD3	V	*4
Input voltage, low	V_{IL}		0		0.2*VDD3	V	*4
Output voltage, high	V_{OH}	IOH = -0.5mA	0.7*VDD3		VDD3	V	*2
Output voltage, low	V_{OL}	IOL = 0.5mA	0.0		0.3*VDD3	V	*2
Leakage current, Input	I_{IL}	VIN = VSS or VDD3	-1.0		1.0	μA	*1 *3
Leakage current, Output	I_{OL}	VIN = VSS or VDD3	-3.0		3.0	μA	*1
Clock frequency	fosc	VDD3=2.8V Temp.=25°C RADJ=11000	228	240	252	kHz	
Voltage Booster Conversion Efficiency of internal power blocks (refer to DC/DC Converter section)							
1st step-up output efficiency	η_{AVDD}	ILOAD=1.0mA VCI=2.8V	90	95		%	
2nd step-up output efficiency	η_{VGH}	ILOAD=0.2mA VCI=2.8V	90	95		%	
	η_{VGL}	ILOAD=0.1mA VCI=2.8V	90	95		%	
3rd step-up output efficiency	η_{VCL}	ILOAD=0.3mA VCI=2.8V	90	95		%	

[Note]

1. Pads under consideration: IM, CSB, E_WRB, RWB_RDB, RS, & DB
2. Pads under consideration: DB
3. At room temperature.
4. Pads under consideration: IM, CSB, E_WRB, RWB_RDB, RS, DB & RESETB

Table 16. DC Characteristics for LCD driver outputs

(AVDD=5.0V, VSS = 0V, T_{OP} = -40°C ~ 85°C).

Parameters	Symbol	Condition		Min.	Typ.	Max.	Unit	Note
On resistance, LCD gate driver output	Ron	VGH–VGL=30.0V, VGH=16.5V, VGL=-13.5V, Vgo=VGH - 0.5V			-	4	kΩ	
Output voltage deviation (Mean value)	ΔVo	SAP=101	4.2V ≤ Vso		±20	±55	mV	
			0.8V < Vso < 4.2V		±10	±30	mV	
			Vso ≤ 0.8V		±20	±55	mV	
LCD source driver output voltage range	Vso	-		0.1	-	GVDD	V	
LCD source driver delay (Cload=18pF, & Rload=11KΩ)	tSD1	AVDD=5.0V, GVDD=4.5V SAP = 010		-	-	80	μs	
	tSD2	AVDD=5.0V, GVDD=4.5V SAP = 011		-	-	50	μs	
	tSD3	AVDD=5.0V, GVDD=4.5V SAP = 100		-	-	40	μs	
	tSD4	AVDD=5.0V, GVDD=4.5V SAP = 101		-	-	30	μs	
Current consumption, Standby mode	I_{stby_VDD3}	Standby mode, VDD3=2.8V, VDD=1.55V, VCI=2.8V		-	-	5	μA	*1 *3
	I_{stby_VDD}			-	-	5	μA	
	I_{stby_VCI}			-	-	10	μA	
Current consumption, Sleep mode	I_{sleep_VDD3}	Sleep mode, VDD3=2.8V, VCI=2.8V		-	-	5	μA	*1 *3
	I_{sleep_VCI}			-	-	45	μA	
Current consumption, Normal operation	I_{VCI}	No load, VDD3=2.8, VCI=2.8V		-	-	3	mA	
	I_{VDD3_RGB}			-	-	150	μA	*4
	I_{VDD3_CPU}					10	μA	
Current consumption, during programming MTP	I_{MTP}	VGH=17V				0.6	mA	*2
	I_{MTP}	VGH=15V				0.6	mA	*2

[Note]

1. At room temperature.
2. Simulation result, with typical conditions: VDD3=2.8, VCI=2.8V.
3. When Standby/Sleep mode, the driver IC do not take any data on DB bus and control pads.
4. CPU access is inactive.

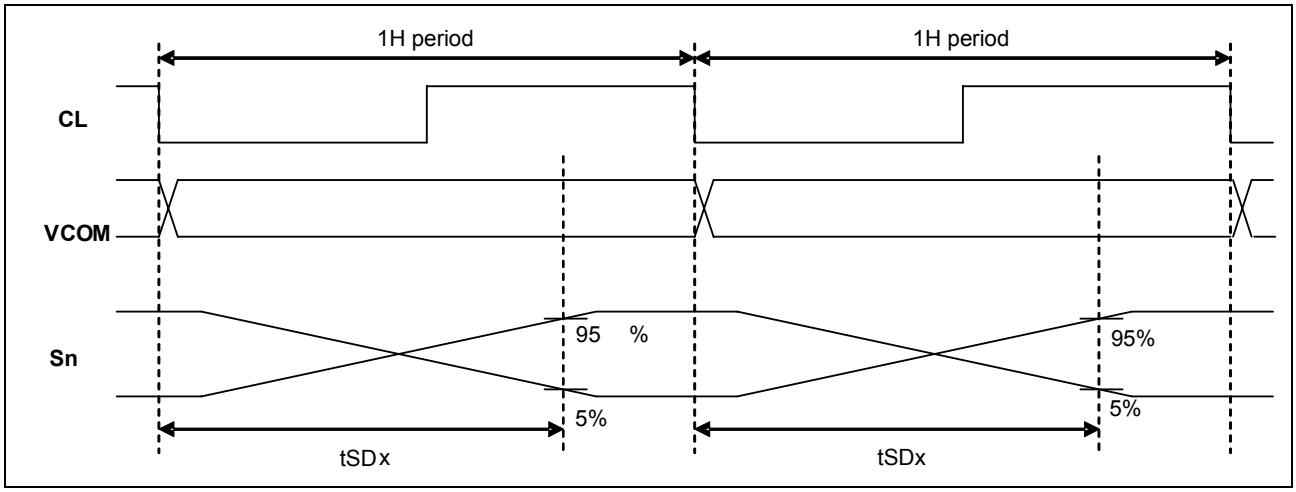
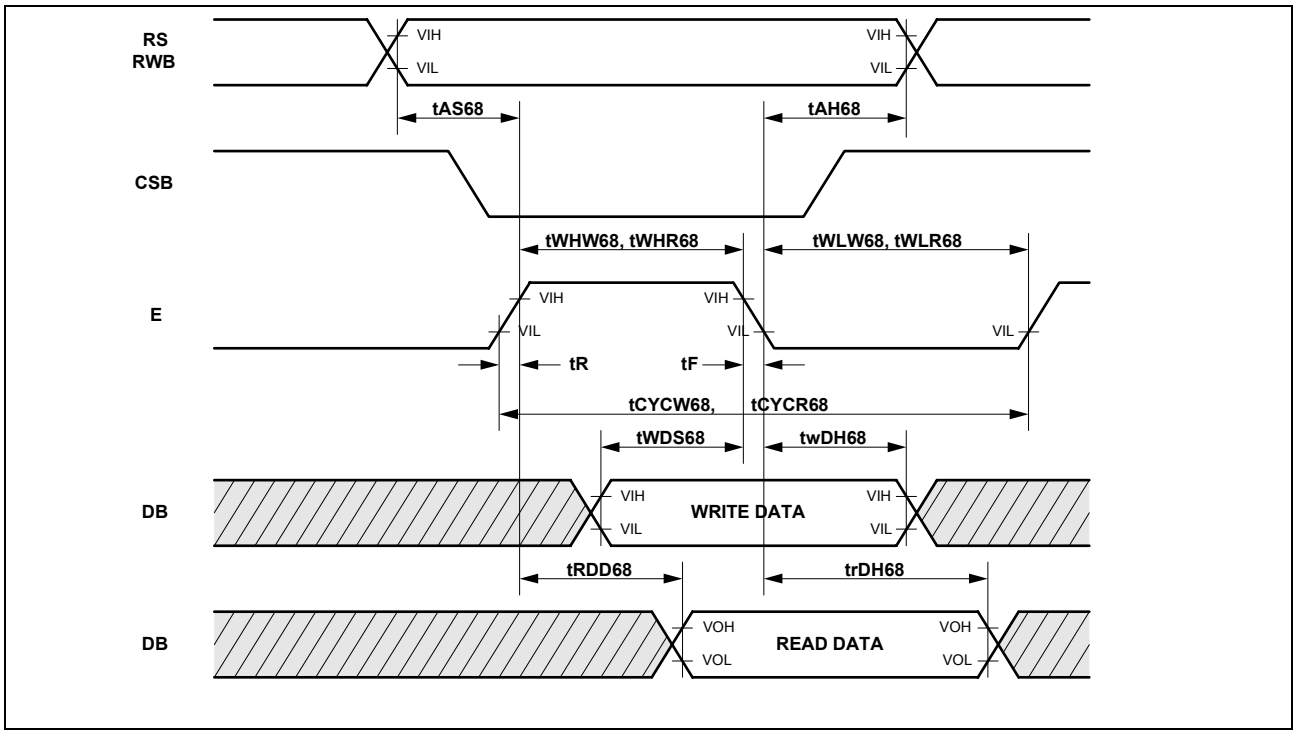


Figure 6. DC characteristics

6.3. AC characteristics

6.3.1. 68-Series 18-/16-/9-/8-bit Interface



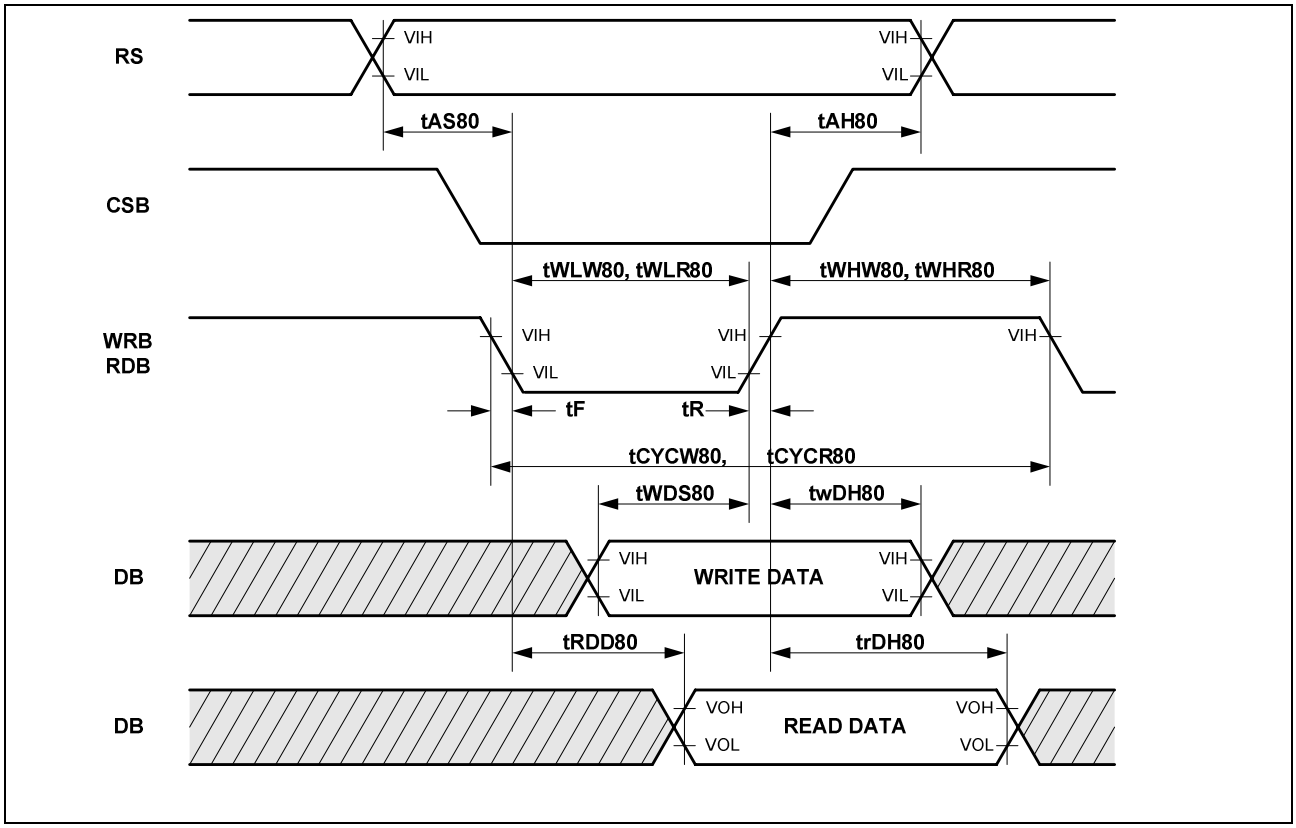
[Note] tWLW68 and tWLR68 are determined by the overlap period of low CSB and high E.

(VDD3=1.6 ~ 3.3V, VSS = 0V, T_{OP}= -40°C ~ 85°C)

Parameter	Description	Min.	Max.	Unit
tCYCW68	Cycle time (Write)	100	-	ns
tCYCR68	Cycle time (Read)	500	-	ns
tR, tF	rise / fall time	-	10	ns
tWLW68	Pulse Width Low (Write)	40	-	ns
tWLR68	Pulse Width Low (Read)	250	-	ns
tWHW68	Pulse Width High (Write)	40	-	ns
tWHR68	Pulse Width High (Read)	200	-	ns
tAS68	RS, RWB to CSB, E setup time	0	-	ns
tAH68	RS, RWB to CSB, E hold time	0	-	ns
tWDS68	Write data setup time	60	-	ns
tWDH68	Write data hold time	2	-	ns
tRDD68	Read data delay time	-	200	ns
tRDH68	Read data hold time	5	-	ns

Figure 7. AC characteristics of 68-Series parallel interface.

6.3.2. 80-Series 18-/16-/9-/8-bit interface



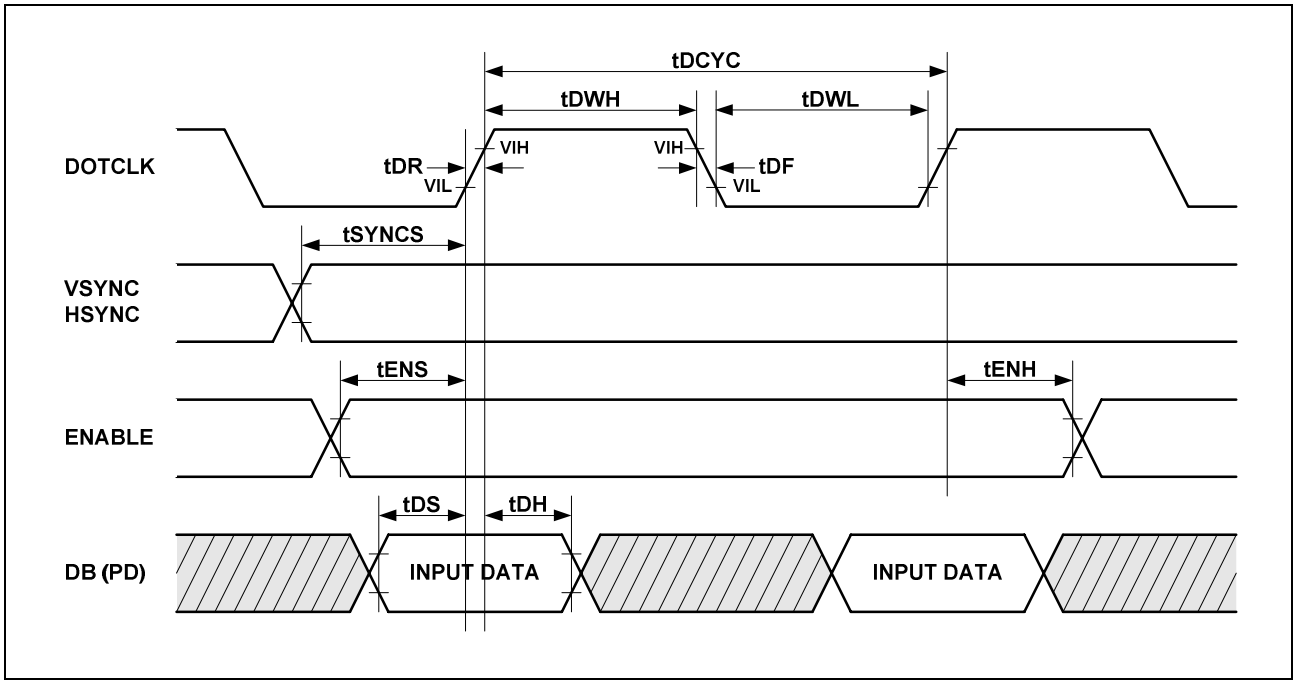
[Note] tWLW80 and tWLR80 are determined by the overlap period of low CSB and low WRB or low CSB and low RDB

(VDD3=1.6 ~ 3.3V, VSS = 0V, T_{OP} = -40°C ~ 85°C)

Parameter	Description	Min.	Max.	Unit
tCYCW80	Cycle time (Write)	100	-	ns
tCYCR80	Cycle time (Read)	500	-	ns
tR, tF	Pulse rise / fall time	-	10	ns
tWLW80	Pulse Width Low (Write)	40	-	ns
tWLR80	Pulse Width Low (Read)	250	-	ns
tWHW80	Pulse Width High (Write)	40	-	ns
tWHR80	Pulse Width High (Read)	200	-	ns
tAS80	RS to CSB, WRB (or RDB) setup time	0	-	ns
tAH80	RS to CSB, WRB (or RDB) hold time	0	-	ns
tWDS80	Write data setup time	60	-	ns
tWDH80	Write data hold time	2	-	ns
tRDD80	Read data delay time	-	200	ns
tRDH80	Read data hold time	5	-	ns

Figure 8. AC characteristics or 80-Series parallel interface.

6.3.3. RGB interface

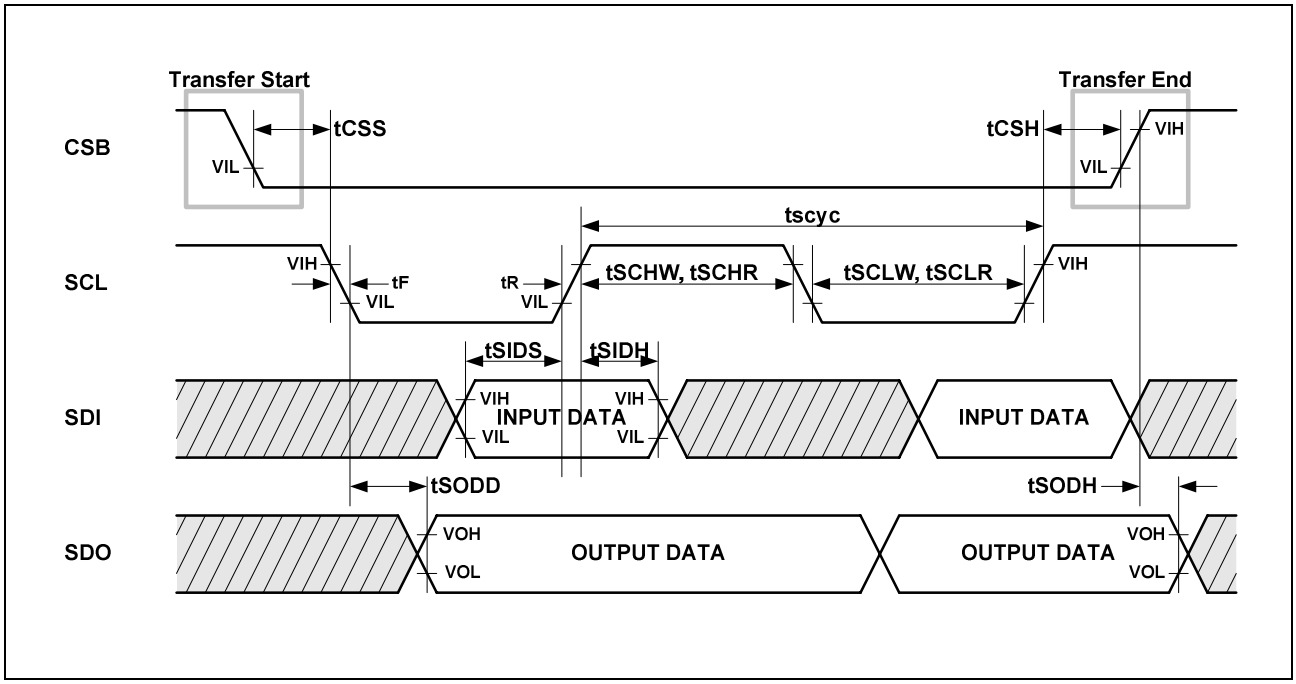


(VDD3=1.6 ~ 3.3V, VSS = 0V, T_{OP} = -40°C ~ 85°C)

Parameter	Description	Min.	Max.	Unit
tDCYC	DOTCLK period	80	-	ns
tDWL	DOTCLK pulse width low	40	-	ns
tDWH	DOTCLK pulse width high	40	-	ns
tDR / tDF	DOTCLK rising / falling time	-	10	ns
tSYNCS	VSYNC, HSYNC setup	0	-	ns
tENS	ENABLE setup	30	-	ns
tENH	ENABLE hold	20	-	ns
tDS	Input Data setup	30	-	ns
tDH	Input Data hold	20	-	ns

Figure 9. AC Characteristics of RGB Interface.

6.3.4. Serial peripheral interface (IM = 4'b010X)

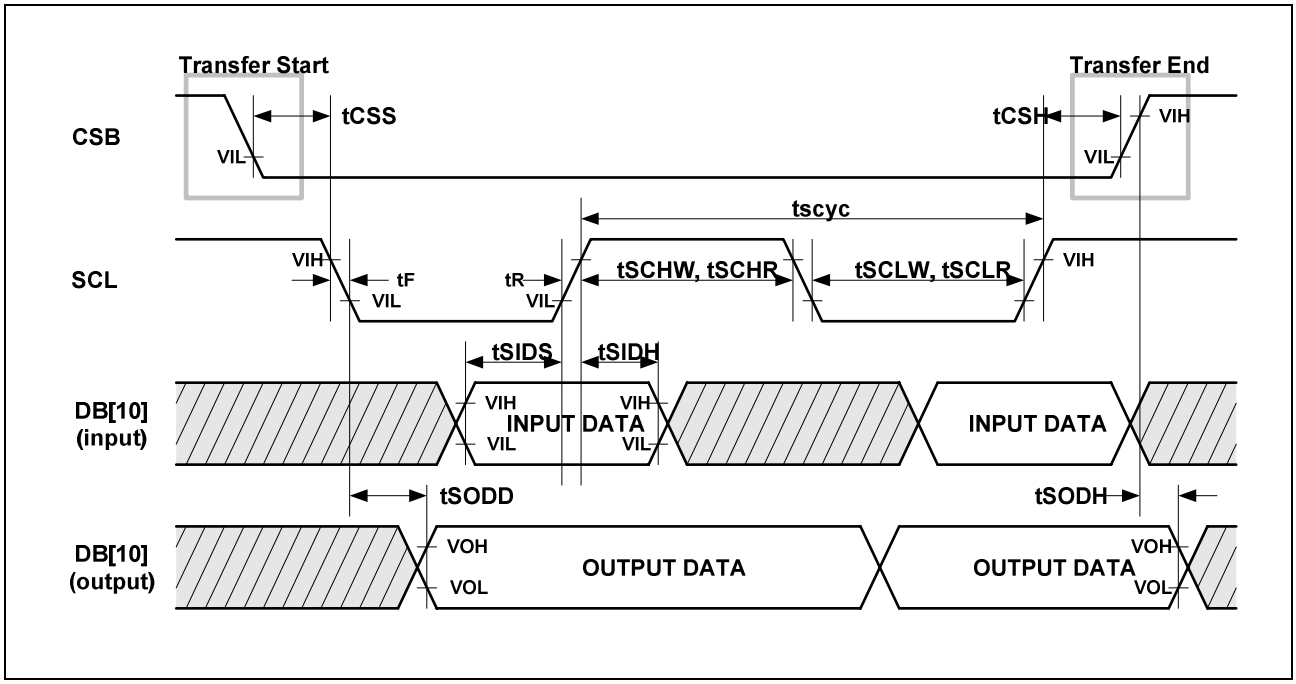


(VDD3=1.6 ~ 3.3V, VSS = 0V, T_{OP} = -40°C ~ 85°C)

Parameter	Description	Min.	Max.	Unit
tscyc (write)	Serial clock write cycle time	100	-	ns
tscyc (read)	Serial clock read cycle time	500	-	ns
tR, tF	Serial clock rise / fall time	-	20	ns
tSCHW	Pulse width high for write	40	-	ns
tSCHR	Pulse width high for read	230	-	ns
tSCLW	Pulse width low for write	60	-	ns
tSCLR	Pulse width low for read	230	-	ns
tCSS	Chip Select setup time	20	-	ns
tCSH	Chip Select hold time	60	-	ns
tSIDS	Serial input data setup time	40	-	ns
tSIDH	Serial input data hold time	30	-	ns
tSODD	Serial output data delay time	-	130	ns
tSODH	Serial output data hold time	5	-	ns

Figure 10. AC characteristics of serial peripheral interface (4-wire).

6.3.5. Serial peripheral interface (IM = 4'b0111)



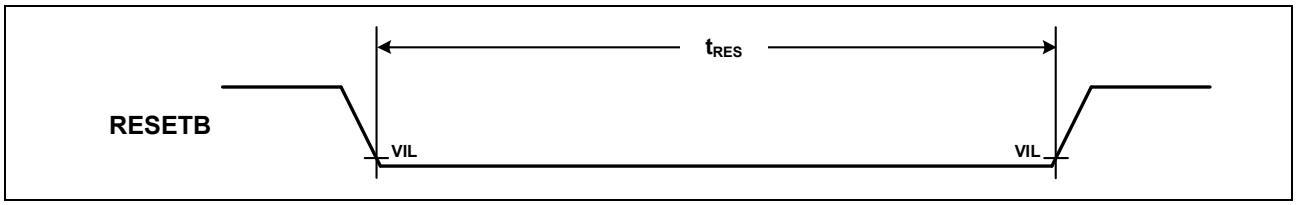
(VDD3=1.6 ~ 3.3V, VSS = 0V, T_{OP} = -40°C ~ 85°C)

Parameter	Description	Min.	Max.	Unit
tscyc (write)	Serial clock write cycle time	67	-	ns
tscyc (read)	Serial clock read cycle time	500	-	ns
tR, tF	Serial clock rise / fall time	-	10	ns
tSCHW	Pulse width high for write	33	-	ns
tSCHR	Pulse width high for read	230	-	ns
tSCLW	Pulse width low for write	34	-	ns
tSCLR	Pulse width low for read	230	-	ns
tCSS	Chip Select setup time	20	-	ns
tCSH	Chip Select hold time	30	-	ns
tSIDS	Serial input data setup time	30	-	ns
tSIDH	Serial input data hold time	30	-	ns
tSODD	Serial output data delay time	-	130	ns
tSODH	Serial output data hold time	5	-	ns

Figure 11. AC characteristics of serial peripheral interface (3-wire).

6.3.6. RESETB signal

The IC is initialized by RESETB input. The signal must be held low for at least 20us. Do not access the GRAM or set the instructions until the R-C oscillation frequency becomes stable after power has been applied(10 ms).



Parameter	Description	Min.	Max.	Unit
tRES	Reset low pulse width	20	-	µs

Figure 12. AC characteristics of RESETB timing

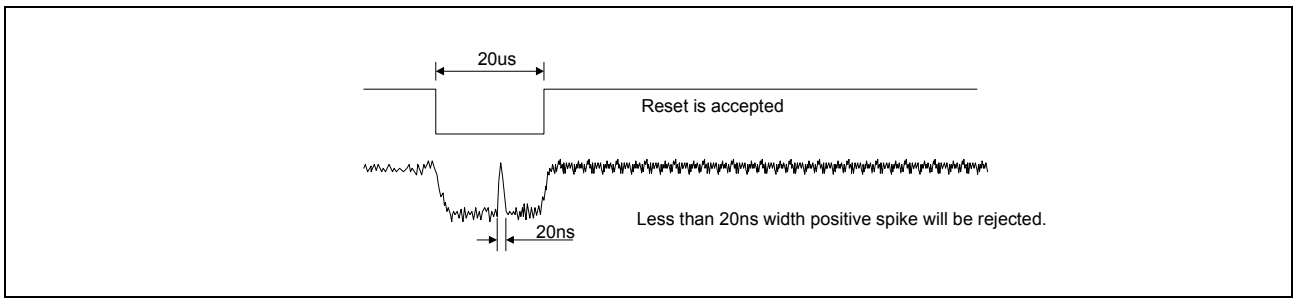
Table 17. Reset operation according to tRES pulse width condition during.

tRES Pulse	Action
Shorter than 7 us	RESETB signal will be ignored [Note].
Longer than 20 us	Reset the IC - All registers are initialized when reset is asserted. - GRAM is not automatically initialized by RESET input so it must be initialized by software while display is off (D=00). - Output driver pad : Source output - VSS level Gate output - VGL level.
Between 7 us and 20 us	Not determined

[Note]

This is done to prevent short transient noises such as glitches, bouncing noises, electrostatic discharges from causing false resets.

User may or may not use RESETB pad. When it is used, user should satisfy the conditions described in the table above. But when RESETB is not in use, this pad should be left unconnected and internally generated POR (Power-On-Reset) is used, instead. Spikes under 20ns in duration will be ignored for a valid reset pulse as shown below:



7. Functional Description

7.1. CPU interface

S6D0151 has 9 high-speed CPU interfaces: 80-Series 18-/16-/9-/8-bit CPU Interfaces (4), 68-Series 18-/16-/9-/8-bit CPU Interfaces (4) and Serial Peripheral Interface, or SPI (1). IM[3:0] signals determine one of 9 interface mode.

A host may write/read data to/from internal GRAM (Graphics RAM) as well as internal control registers through these CPU interfaces.

All instructions except oscillation start can be performed with 0-cycle, so the instructions can be written in succession.

When a host wants to access the drive IC, it must generate control signals as shown below.

Table 18. Register selection in case of 80/68-Series 8-/9-/16-/18-bit CPU Interface mode.

E / WRB	RWB / RDB	RS	Operations
1 / 0	0 / 1	0	Write indexes into IR (Index Register).
1 / 1	1 / 0	0	Read internal status.
1 / 0	0 / 1	1	Write into control registers or GRAM.
1 / 1	1 / 0	1	Read data from control registers or GRAM.

Table 19. Register selection in case of Serial Peripheral Interface mode.

RWB Bit	RS Bit	Operations
0	0	Write indexes into IR (Index Register).
1	0	Read internal status.
0	1	Write into control registers or GRAM.
1	1	Read data from control registers or GRAM.

7.2. RGB interface

RGB interface can be selected to display a motion picture on the panel. When the RGB interface is selected, a set of the synchronization signals (VSYNC, HSYNC, and DOTCLK) will be actived for the display operation. The data on DB[17:0] are written in combination of ENABLE and DOTCLK. This allows flicker-free update of screen.

7.3. Command box

S6D0151 has a command box to control internal operations and many internal analog blocks including power blocks, source driver and gate array.

7.4. Graphics RAM

The graphics RAM (GRAM) stores 18-bits/pixel data totaling the bit-pattern data of 128-RGB x 160 pixels.

There is an address counter for GRAM access. The address counter (AC) points addresses to the GRAM. With an address set instruction, the address from CPU interface is stored into AC. Once the data is written into GRAM, the address stored at AC is automatically increased (or decremented) by 1. But when reading data from GRAM, the AC is not updated. Window Address Function allows data to be written only into the Window specified by some control registers.

7.4.1. GRAM address map

The image data stored in GRAM corresponds to real pixel on display as shown below.

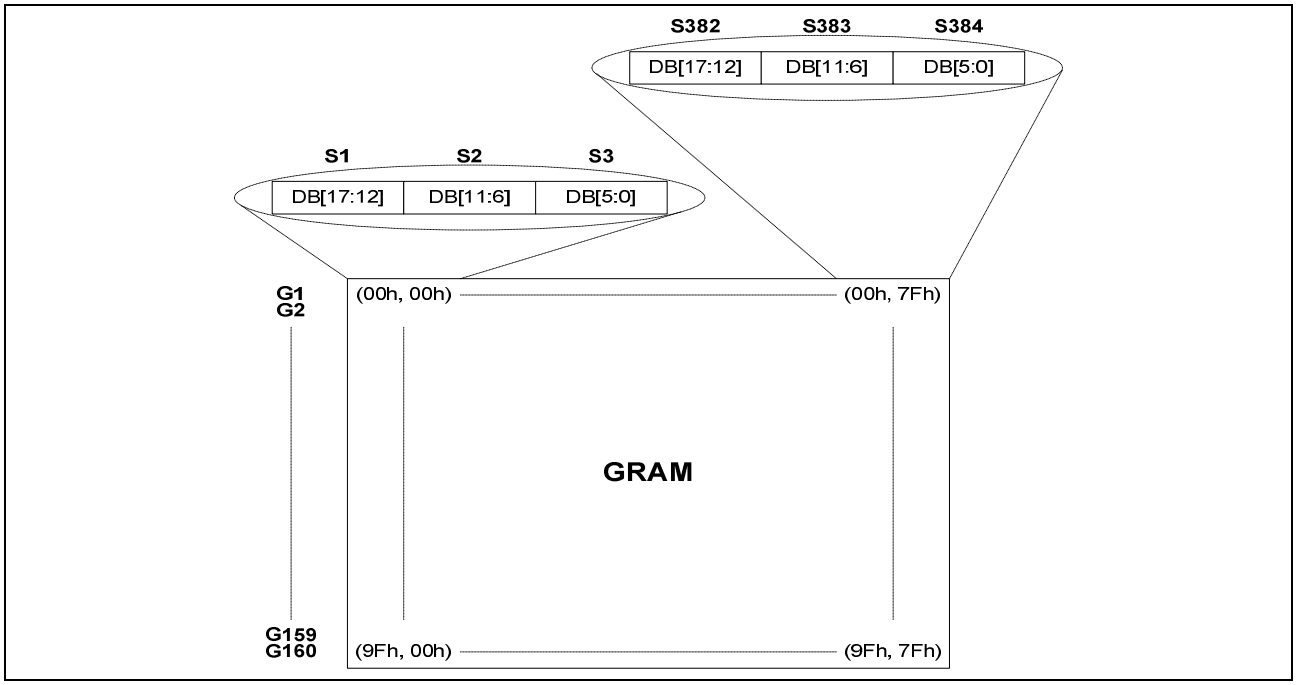


Figure 13. GRAM address and display image.

[Note] The display condition of this figure is SS = 0, BGR = 0, GS = 0.

7.5. Panel I/F timing controller

The Panel Interface Controller generates timing signals for TFT-LCD Driver and control signals for the operation of internal circuits such as source driver and GRAM. The GRAM read operations are done by this Panel Interface Controller and GRAM write operations are done through system interface. They are performed independently to avoid the interference between them.

7.6. Grayscale voltage generator

The grayscale voltage circuit generates a certain voltage level that is specified by the grayscale ϒ-adjusting resistor for LCD driver circuit. By use of the generator, 262,144 colors can be displayed at the same time. For details, refer to Gamma-Adjustment Function section.

7.7. Oscillator (OSC)

The S6D0151 provides a R-C oscillator without requiring any external resistor. The appropriate oscillator clock frequency for operating voltage, display size, and frame frequency can be obtained by adjusting the register setting value [R61h]. A clock source can also be supplied externally. Since the R-C oscillator suspends operating during the standby mode, the current consumption can be reduced. For details, refer to Oscillation Circuit section.

7.8. Source driver array

The source driver array consists of 384 drivers (S1 through S384). Display data is latched when all 384-ch data has arrived. The source drivers, then, take the latched data and convert them into a certain level of analog voltage potential. SS bit can switch the shift direction of array data.

7.9. Gate drivers

The gate driver consists of 160 gate drivers (G1 to G160). VGH or VGL level is chosen by the signal from the gate control circuit.

8. Instruction Sets

8.1. Introduction

S6D0151 uses 18-bit bus architecture. To execute an instruction, the control information from external 18-/16-/9-/8-bit data is stored in Index Register (IR) and Control Register (CR) as will be described later to allow high-speed interface to high-performance microcomputer.

The internal operation of S6D0151 is determined by the signals sent from microcomputer. These signals, which include the register selection signal (RS), the write/read signals (E/RWB for 68-Series, WRB/RDB for 80-Series), and the internal 16-bit data bus signals (IB15 to IB0), make up the S6D0151 instructions.

There are eight categories of instructions as follows:

Specifies the index
- Reads the status
- Controls the display
- Controls power
- Processes the graphics data
- Sets internal GRAM addresses
- Transfers data to and from the internal GRAM
- Sets grayscale level for the internal grayscale palette table

Normally, the instructions for writing data are used the most frequently. As a result, the automatic update of the internal GRAM address after each data write can lighten the microcomputer's load. Because instructions are executed in 0 cycles, they can be written in succession.

The 16-bit instruction assignment varies with interface mode specified by IM. The assignment for each interface mode in described later in System Interface section.

8.2. Instruction set

Table 20. Instruction set table (I)

Reg.No	R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0	Register Name / Description
IR	W	0	X	X	X	X	X	X	X	X	ID7	ID6	ID5	ID4	ID3	ID2	ID1	ID0	**Index /** Sets the index register value
SR	R	0	L7	L6	L5	L4	L3	L2	L1	L0	0	0	0	0	0	0	0	0	**Status read /** Reads the internal status of the S6D0151
R00h	W	1	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	1	**Start Oscillation(R00H) /** Starts/Stops the oscillation circuit
	R	1	0	0	0	0	0	0	0	1	0	1	0	1	0	0	0	1	**Device code read /** Read 0151H
R01h	W	1	X	X	X	DPL (0)	EPL (0)	SM (0)	GS (0)	SS (0)	X	X	X	NL4 (1)	NL3 (0)	NL2 (1)	NL1 (0)	NL0 (0)	**Driver output control(R01H) /** DPL: set polarity of DOTCLK pad while using RGB interface. EPL: set polarity of ENABLE pad while using RGB interface. SM: gate driver division drive control GS: gate driver shift direction SS: source driver shift direction NL4-0: number of driving lines
R02h	W	1	X	X	X	X	X	X	FL1 (0)	FL0 (0)	X	X	X	FLD (0)	X	X	X	X	**LCD-Driving-waveform control (R02H)/** FL1-0 : Line/Frame inversion setting FLD : Interface Mode Control
R03h	W	1	X	X	X	BGR (0)	X	X	MDT1 (0)	MDT0 (0)	X	X	I/D1 (1)	I/D0 (1)	AM (0)	X	X	X	**Entry mode(R03H) /** BGR: RGB swap control MDT2-1: Multiple Data Transfer I/D1-0: address counter Increment / Decrement control AM: horizontal / vertical RAM update
R07h	W	1	X	X	X	PT1 (0)	PT0 (0)	X	X	SPT (0)	X	X	GON (0)	DTE (0)	CL (0)	REV (0)	D1 (0)	D0 (0)	**Display control (R07H) /** PT1-0: Non-display area source output control SPT: 1st /2nd partial display enable GON: gate-off to be VSS level DTE:DISPTMG to be VSS level CL: 8-color display mode enable REV: display area inversion drive D1-0: source output control
R08h	W	1	X	X	X	X	FP3 (0)	FP2 (0)	FP1 (1)	FP0 (0)	X	X	X	X	BP3 (0)	BP2 (0)	BP1 (1)	BP0 (0)	**Blank period control 1 (R08H)/** BP3-0: Back porch setting FP3-0: Front porch setting
R0Bh	W	1	X	X	X	X	X	X	DIV1 (0)	DIV0 (0)	X	X	X	X	RTN3 (0)	RTN2 (0)	RTN1 (0)	RTN0 (0)	**Frame cycle control (R0BH)/** DIV1-0: division ratio of internal clock setting RTN3-0: set the 1-H period
R0Ch	W	1	X	X	X	X	X	X	X	RM (0)	X	X	DM1 (0)	DM0 (0)	X	X	RIM1 (0)	RIM0 (0)	**External interface control(R0CH) /** RM: specify the interface for RAM access DM1-0: specify display operation mode RIM1-0: specify RGB-I/F mode
R10h	W	1	X	X	SAP2 (0)	SAP1 (0)	SAP0 (0)	BT2 (0)	BT1 (0)	BT0 (0)	DC2 (0)	DC1 (0)	DC0 (0)	AP2 (0)	AP1 (0)	AP0 (0)	SLP (0)	STB (0)	**Power control 1 (R10H) /** SAP2-0: Adjust the amount of fixed current in the op Amp for the source driver BT2-0: Adjust scale factor of the step-up DC2-0: Select operating frequency in the step-up circuit AP2-0: Adjust the amount of fixed current in the op Amp for the power supply SLP: enters the sleep mode STB: enters the standby mode
R11h	W	1	VR1C (0)	X	X	VRN14 (0)	VRN13 (0)	VRN12 (0)	VRN11 (0)	VRN10 (0)	X	X	X	VRP14 (0)	VRP13 (0)	VRP12 (0)	VRP11 (0)	VRP10 (0)	**Gamma control 1 (R11H)/** VR1C : Control step of amplitude positive and negative of 64-grayscale VRN14-10: Control amplitude (positive polarity) of 64-grayscale. VRP14-10: Control amplitude (negative polarity) of 64-grayscale.
R12h	W	1	X	X	X	X	X	X	X	X	SVC3 (0)	SVC2 (0)	SVC1 (0)	SVC0 (0)	X	0	VRH5 (0)	VRH4 (0)	**Power control 2 / SVC3-0:**set VCI1 voltage **Power control 3 /** VRH5-4 : Set GVDD voltage
R13h	W	1	X	X	X	X	VCMR (1)	X	X	X	X	X	X	PON (0)	VRH3 (0)	VRH2 (0)	VRH1 (0)	VRH0 (0)	**Power control 3 /** VCMR : select VCOMH voltage adjusting method PON : Power circuit ON/OFF setting VRH3-0 : Set GVDD voltage
R14h	W	1	X	VDV6 (0)	VDV5 (0)	VDV4 (0)	VDV3 (0)	VDV2 (0)	VDV1 (0)	VDV0 (0)	VCOM G (0)	VCM6 (0)	VCM5 (0)	VCM4 (0)	VCM3 (0)	VCM2 (0)	VCM1 (0)	VCM0 (0)	**Power control 4 /** VCOMG : VCOML voltage level negative voltage setting VDV6-0 : COM output amplitude setting VCM6-0 : VCOMH voltage level setting
R21h	W	1	AD15 (0)	AD14 (0)	AD13 (0)	AD12 (0)	AD11 (0)	AD10 (0)	AD9 (0)	AD8 (0)	AD7 (0)	AD6 (0)	AD5 (0)	AD4 (0)	AD3 (0)	AD2 (0)	AD1 (0)	AD0 (0)	**RAM address register /** AD15-AD0
R22h	W	1	WD15	WD14	WD13	WD12	WD11	WD10	WD9	WD8	WD7	WD6	WD5	WD4	WD3	WD2	WD1	WD0	**Write data to GRAM /** WD15-WD0
	R	1	RD15	RD14	RD13	RD12	RD11	RD10	RD9	RD8	RD7	RD6	RD5	RD4	RD3	RD2	RD1	RD0	**Read data from GRAM /** RD15-RD0
R30h	W	1	X	X	X	X	X	PKP12 (0)	PKP11 (0)	PKP10 (0)	X	X	X	X	X	PKP02 (0)	PKP01 (0)	PKP00 (0)	**Gamma control 2/** PKP12-10, PKP02-00: Micro adjustment setting
R31h	W	1	X	X	X	X	X	PKP32 (0)	PKP31 (0)	PKP30 (0)	X	X	X	X	X	PKP22 (0)	PKP21 (0)	PKP20 (0)	**Gamma control 2/** PKP32-30, PKP22-20: Micro adjustment setting
R32h	W	1	X	X	X	X	X	PKP52 (0)	PKP51 (0)	PKP50 (0)	X	X	X	X	X	PKP42 (0)	PKP41 (0)	PKP40 (0)	**Gamma control 2/** PKP52-50, PKP42-40: Micro adjustment setting
R33h	W	1	X	X	X	X	X	PRP12 (0)	PRP11 (0)	PRP10 (0)	X	X	X	X	X	PRP02 (0)	PRP01 (0)	PRP00 (0)	**Gamma control 2/** PRP12-10, PRP02-00: Gradient adjustment setting
R34h	W	1	X	X	X	X	X	PKN12 (0)	PKN11 (0)	PKN10 (0)	X	X	X	X	X	PKN02 (0)	PKN01 (0)	PKN00 (0)	**Gamma control 2/** PKN12-10, PKN2-0: Micro adjustment setting
R35h	W	1	X	X	X	X	X	PKN32 (0)	PKN31 (0)	PKN30 (0)	X	X	X	X	X	PKN22 (0)	PKN21 (0)	PKN20 (0)	**Gamma control 2/** PKN32-30, PKN22-20: Micro adjustment setting
R36h	W	1	X	X	X	X	X	PKN52 (0)	PKN51 (0)	PKN50 (0)	X	X	X	X	X	PKN42 (0)	PKN41 (0)	PKN40 (0)	**Gamma control 2/** PKN52-50, PKN42-40: Micro adjustment setting
R37h	W	1	X	X	X	X	X	PRN12 (0)	PRN11 (0)	PRN10 (0)	X	X	X	X	X	PRN02 (0)	PRN01 (0)	PRN00 (0)	**Gamma control 2/** PRN12-10, PRN02-00: Gradient adjustment setting
R38h	W	1	X	X	X	X	VRN03 (0)	VRN02 (0)	VRN01 (0)	VRN00 (0)	X	X	X	X	VRP03 (0)	VRP02 (0)	VRP01 (0)	VRP00 (0)	**Gamma control 3/** VRN03-00 : gamma amplitude setting(negative polarity) VRP03-00 : gamma amplitude setting(positive polarity)
R40h	W	1	X	X	X	X	X	X	X	X	X	X	X	SCN4 (0)	SCN3 (0)	SCN2 (0)	SCN1 (0)	SCN0 (0)	**Gate Scan Position /** SCN4-0 : scan starting position of gate
R42h	W	1	SE17 (1)	SE16 (0)	SE15 (0)	SE14 (1)	SE13 (1)	SE12 (1)	SE11 (1)	SE10 (1)	SS17 (0)	SS16 (0)	SS15 (0)	SS14 (0)	SS13 (0)	SS12 (0)	SS11 (0)	SS10 (0)	**1st screen driving position/** SE17-10 : 1st screen end position setting SS17-10 : 1st screen start position setting
R43h	W	1	SE27 (1)	SE26 (0)	SE25 (0)	SE24 (1)	SE23 (1)	SE22 (1)	SE21 (1)	SE20 (1)	SS27 (0)	SS26 (0)	SS25 (0)	SS24 (0)	SS23 (0)	SS22 (0)	SS21 (0)	SS20 (0)	**2nd screen driving position/** SE27-20 : 2nd screen end position setting SS27-20 : 2nd screen start position setting
R44h	W	1	HEA7 (0)	HEA6 (1)	HEA5 (1)	HEA4 (1)	HEA3 (1)	HEA2 (1)	HEA1 (1)	HEA0 (1)	HSA7 (0)	HSA6 (0)	HSA5 (0)	HSA4 (0)	HSA3 (0)	HSA2 (0)	HSA1 (0)	HSA0 (0)	**Horizontal window address/** HEA7-0 : Horizontal window address end position HSA7-0 : Horizontal window address start position
R45h	W	1	VEA7 (1)	VEA6 (0)	VEA5 (0)	VEA4 (1)	VEA3 (1)	VEA2 (1)	VEA1 (1)	VEA0 (1)	VSA7 (0)	VSA6 (0)	VSA5 (0)	VSA4 (0)	VSA3 (0)	VSA2 (0)	VSA1 (0)	VSA0 (0)	**Vertical window address/** VEA7-0 : Vertical window address end position VSA7-0 : Vertical window address start position

Table 21. Instruction set table (II)

Reg. No	R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0	Register Name / Description
R61h	W	1	X	X	X	X	X	X	X	0	X	X	X	RADJ4 (1)	RADJ3 (1)	RADJ2 (0)	RADJ1 (0)	RADJ0 (0)	Sets internal oscillator oscillation frequency (RADJ4-0)
R69h	W	1	X	X	X	X	X	X	X	X	X	X	X	NLDC3 (0)	NLDC2 (1)	NLDC1 (1)	NLDC0 (0)	NLPM (0)	Low power mode (LPM) setting register NLPM : Sets Low power mode NLDC1-0 : Sets DC/DC converter clock for AVDD at LPM NLDC3-2 : Sets DC/DC converter clock for VGH/L at LPM Select capability of DC/DC converter for VGH/L (NLPDC)
R70h	W	1	X	X	X	X	X	X	X	X	SDT1 (0)	SDT0 (0)	X	X	X	X	EQ1 (0)	EQ0 (0)	Sets source output pre-driving period EQ1-0 : Specifies equalize period SDT1-0 : Specifies source output delay term
R71h	W	1	X	X	X	X	GNO1 (0)	GNO0 (0)	X	X	X	X	X	X	X	X	X	X	Sets the amount of non-overlap period of gate outputs
R72h	W	1	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	SR(1)	Software Reset Control
R73h	W	1	X	X	X	X	X	X	X	X	TEST_KEY7 (0)	TEST_KEY6 (0)	TEST_KEY5 (0)	TEST_KEY4 (0)	TEST_KEY3 (0)	TEST_KEY2 (0)	TEST_KEY1 (0)	TEST_KEY0 (0)	Test Key to update MTP Value. 'hA5 should be written to do it.
RB3h	W	1	X	0	0	0	X	0	1	0	X	X	X	DCR_EX (0)	X	X	X	1	DCR_EX Select Source of Pumping Clock
RB4h	W	1	X	X	X	MTP_SEL (1)	X	X	X	MTP_INIT (0)	X	X	X	MTP_WRB (1)	X	X	X	MTP_LOAD (0)	MTP Control Registers
RB6h	W	1	TEST_IN4	TEST_IN3	SD_EN (0)	SD3 (0)	SD2 (0)	SD1 (0)	PSMD 1 (0)	PSDM 0 (1)	X	X	1	1	1	1	1	1	TEST_IN4-3 : Module Maker Information Power on sequence control of Step-up circuit
RBDh	R/W	1	X	X	X	X	X	X	X	DISEN (0)	X	MTP_DOUT6	MTP_DOUT5	MTP_DOUT4	MTP_DOUT3	MTP_DOUT2	MTP_DOUT1	MTP_DOUT0	DISEN : VGL/VCL Discharge Enable MTP Read Registers.
RBEh	W	1	X	X	X	X	X	X	X	X	X	X	X	IM_SEL (0)	IM_3 (0)	X	X	FLM_MSK (0)	IM_SEL, IM_3 : Interface mode selection FLM_MSK : FLM signal(TEST_OUT[0]) off_switch

8.3. Description of instructions

8.3.1. Index Register (IR)

The index instruction specifies indexes. It can set the register number in the range of 00000000b to 10111110b in binary form. However, do not access index registers and instruction bits that are not allocated in this document.

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	0	*	*	*	*	*	*	*	*	ID7	ID6	ID5	ID4	ID3	ID2	ID1	ID0

8.3.2. Status Read

The status read instruction allows the read operation of internal status of S6D0151. The status indicates the position of horizontal line currently being driven.

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
R	0	L7	L6	L5	L4	L3	L2	L1	L0	0	0	0	0	0	0	0	0

8.3.3. System Control (R00h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	1
R	1	0	0	0	0	0	0	0	1	0	1	0	1	0	0	0	1

Issuing this instruction forces the internal oscillator to start generating clock pulses. It can be used to restart the internal oscillator from the halt state at standby mode. After issuing this instruction, wait at least 10 ms for oscillation to stabilize before issuing the next instruction.
(Refer to Sequence of Standby/Sleep Mode section.)

If this register (00h) is read forcibly, 0151h will be read.

8.3.4. Driver Output Control (R01h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	X	X	X	DPL	EPL	SM	GS	SS	X	X	X	NL4	NL3	NL2	NL1	NL0

DPL

Determine the active polarity of DOTCLK for using RGB interface.

Table 22. DPL and DOTCLK polarity

DPL	DOTCLK	Description
0 (1)	↑ (↓)	Valid (Valid)
0 (1)	↓ (↑)	Invalid (Invalid)

EPL

Determine the active polarity of ENABLE for using RGB interface.

Table 23. EPL, ENABLE and RAM access

EPL	ENABLE	RAM Write	RAM Address
0 (1)	0 (1)	Valid (Valid)	Updated (Updated)
0 (1)	1 (0)	Invalid (Invalid)	Hold (Hold)

SM

Selects the division drive method of the gate driver. When SM = 0, even/odd division is selected; SM = 1, upper/lower division drive is selected. Various connections between TFT panel and the IC can be supported with the combination of SM and GS bit.

GS

Sets the order of Gate Clock generation. When GS = 0, G1 is outputted first and G160 is outputted last. When GS = 1, G160 is outputted first and G1 is outputted last (NL = 5'b10100). But in case of NL = 5'b00001, when GS = 0, G1 is outputted first and G8 is outputted last, and when GS = 1, G8 is outputted first and G1 outputted last

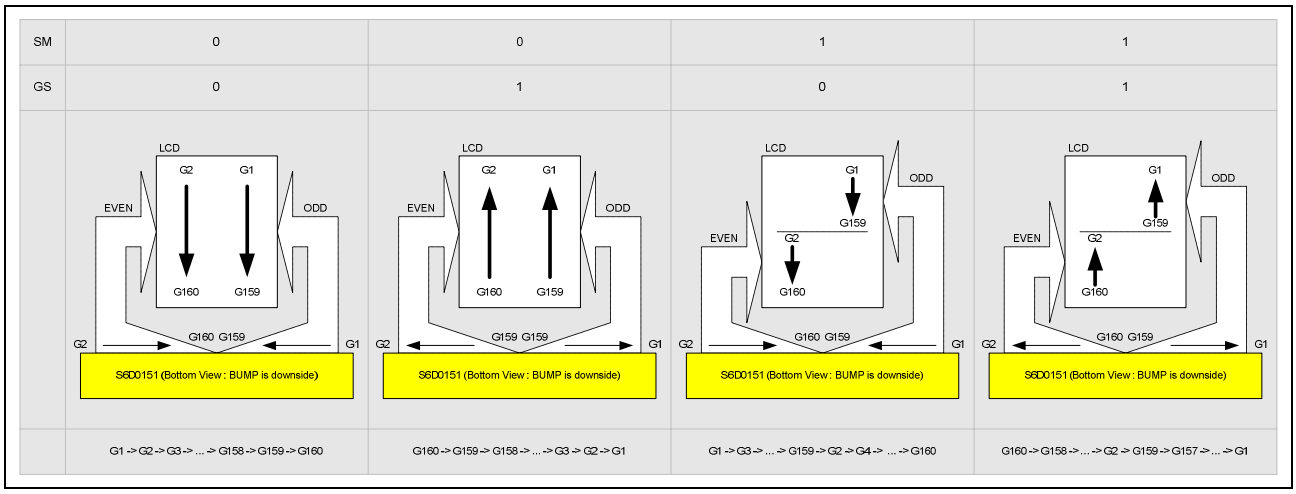


Figure 14. Gate clock generation order selection using GS and SM
(NL = 5'b10100, SCN = 5'b00000)

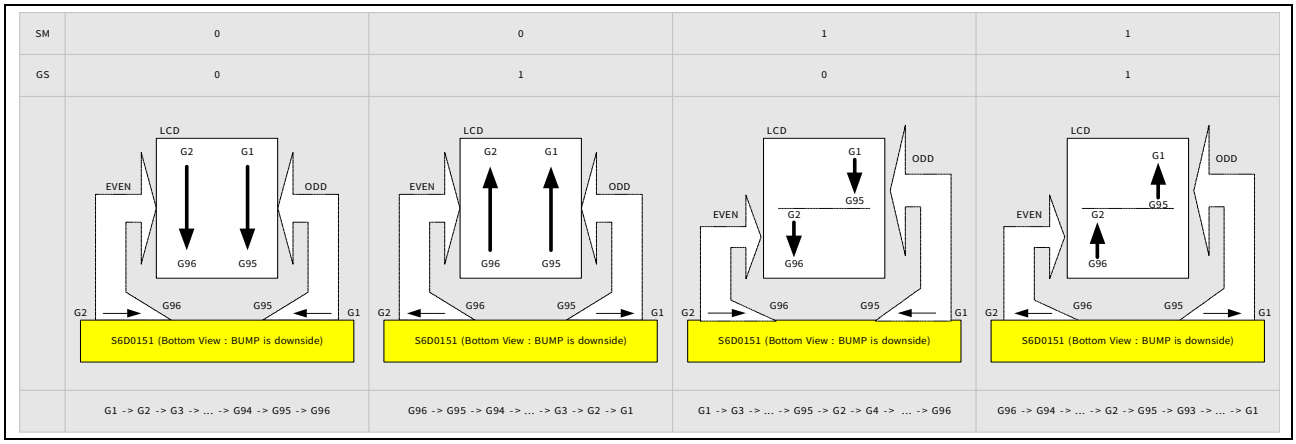


Figure 15. Gate clock generation order selection using GS and SM
(GS = 0 : NL = 5'b01100, SCN = 5'b00000) / (GS = 1 : NL = 5'b01100, SCN = 5'b01000)

SS

Selects the direction of the source driver channel in pixel unit. When user changes the value of SS, memory should be updated to apply the change.

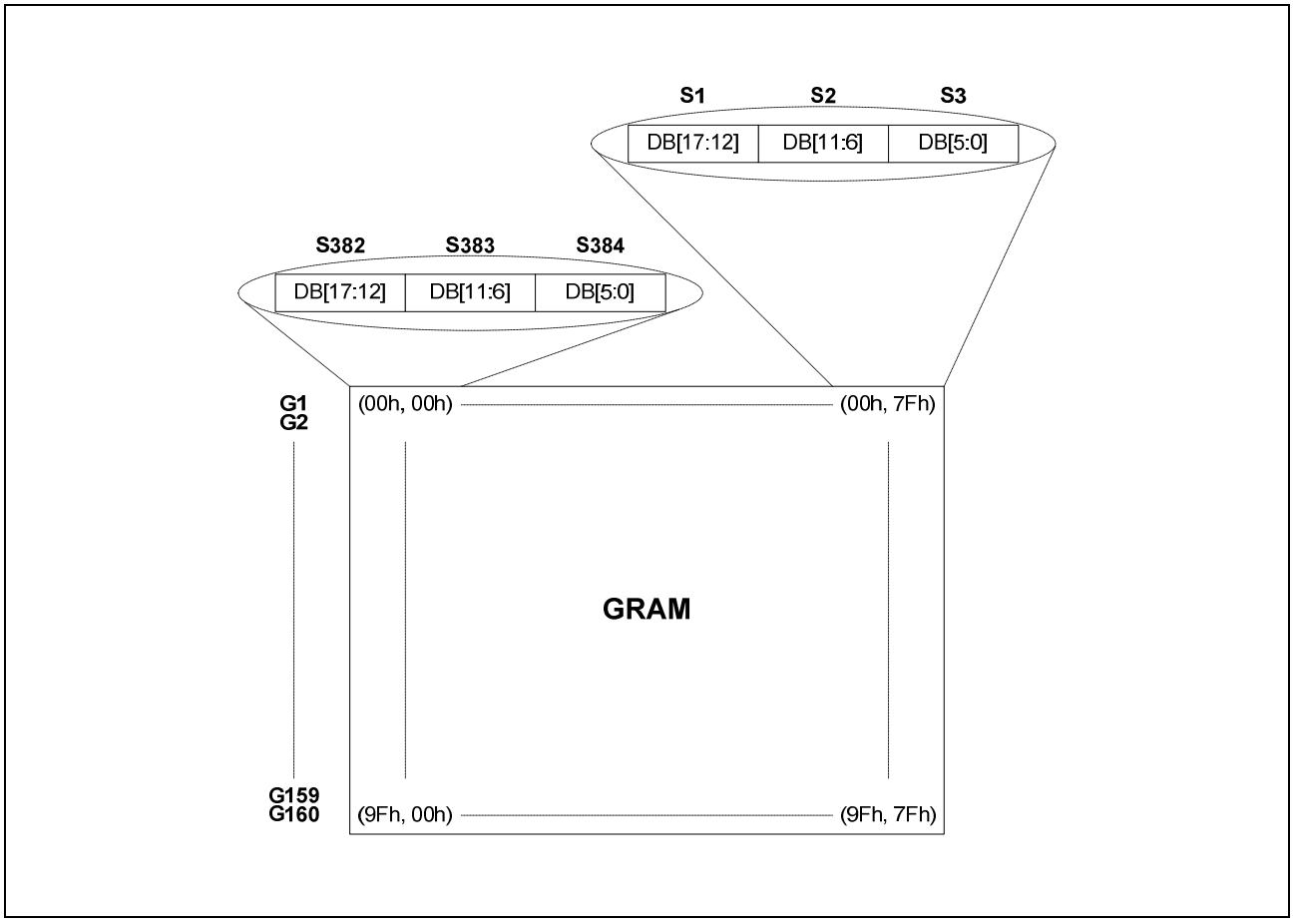


Figure 16. Image mirroring using SS register (SS = 1).

[Note]

The display condition of this figure is SS = 1, BGR = 0, GS = 0.

NL

Specifies the number of horizontal lines to be driven. The number of the lines can be adjusted in units of eight. GRAM address mapping is independent of this setting. The set value should be higher than the panel size. Do not change the setting of NL[4:0] in DISPLAY ON STATE.

Table 24. NL bit and Drive Duty (SCN = 00000)

NL[4:0]	Display Size	Drive Line	Gate Driver- Lines Used
00000	Reserved		
00001	384 X 8 dots	8	G1 to G8
00010	384 X 16 dots	16	G1 to G16
00011	384 X 24 dots	24	G1 to G24
00100	384 X 32 dots	32	G1 to G32
00101	384 X 40 dots	40	G1 to G40
00110	384 X 48 dots	48	G1 to G48
00111	384 X 56 dots	56	G1 to G56
01000	384 X 64 dots	64	G1 to G64
01001	384 X 72 dots	72	G1 to G72
01010	384 X 80 dots	80	G1 to G80
01011	384 X 88 dots	88	G1 to G88
01100	384 X 96 dots	96	G1 to G96
01101	384 X 104 dots	104	G1 to G104
01110	384 X 112 dots	112	G1 to G112
01111	384 X 120 dots	120	G1 to G120
10000	384 X 128 dots	128	G1 to G128
10001	384 X 136 dots	136	G1 to G136
10010	384 X 144 dots	144	G1 to G144
10011	384 X 152 dots	152	G1 to G152
10100	384 X 160 dots	160	G1 to G160

[Note] FP (front porch) and BP (back porch) periods will be inserted as blanking periods (All gates output VGL level) before / after the driver goes through all of the scans.

8.3.5. LCD Inversion Control (R02h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	X	X	X	X	X	X	FL1	FL0	X	X	X	FLD	X	X	X	X

FL / FLD

Set LCD inversion method is shown below. Enables or disables 3-field interlaced scanning function like below. To save power, enable 3 field interlaced scanning function. The 3-field interlaced scanning function is properly operated in FP=2 and SM=0 settings.

Table 25. LCD inversion selection / Interlaced scanning method control.

FL[1:0]	FLD	Description
00	0	Frame Inversion – 1 field interlace
	1	Frame Inversion – 3 field interlace
01	0	Line Inversion – 1 field interlace
	1	Line Inversion – 3 field interlace
10	0	No Inversion. Active with positive polarity (VCOM = Low)
	1	Not available
11	0	No Inversion. Active with negative polarity (VCOM = High)
	1	Not available

For more detail information about inversion, refer to Panel Control Interface section, which will be described later.

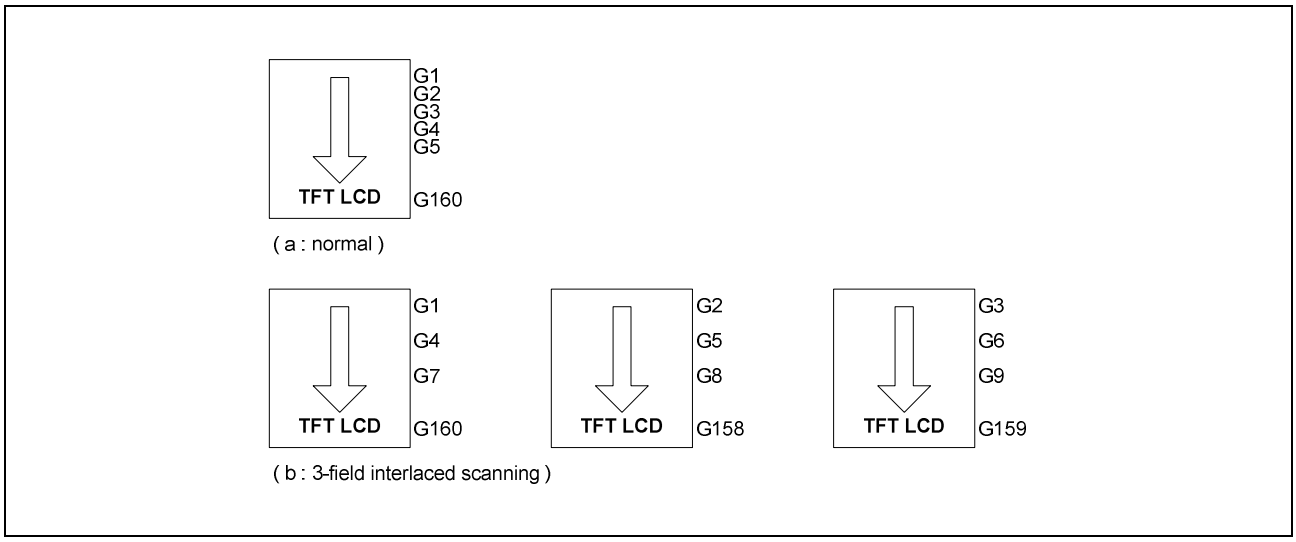


Figure 17. Interlaced scanning methods.

8.3.6. Entry Mode (R03h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	X	X	X	BGR	X	X	MDT1	MDT0	X	X	ID1	ID0	AM	X	X	X

BGR

When 18-bit data is written to GRAM through DB bus, RGB assignment can be changed.

- BGR = 0 ; {DB[17:12], DB[11:6], DB[5:0]} is assigned to {R, G, B}. Actually the analog value that corresponds to DB[17:12] will be outputted first at the source output
- BGR = 1 ; {DB[17:12], DB[11:6], DB[5:0]} is assigned to {B, G, R}. Actually the analog value that corresponds to DB[5:0] will be outputted first at the source output.

MDT

When user wants to transfer 260k color data on 8/16-bit parallel bus, MDT (Multiple Times Data Transfer mode control) register may be used. Set MDT[1:0]=0X(Normal transfer) before reading the Chip code or issuing a MTP read instruction.

Table 26. Multiple Data Transfer Mode Control

MDT[1:0]	IM[3:0]	Description
0X	X	Normal Data Transfer
10	8-bit	260k color data is transferred by 3-times Data Transfer.
	16-bit	260k color data is transferred by 2-times Data Transfer.
11	8-bit	65k color data is transferred by 3-times Data Transfer.
	16-bit	260k color data is transferred by 2-times Data Transfer.

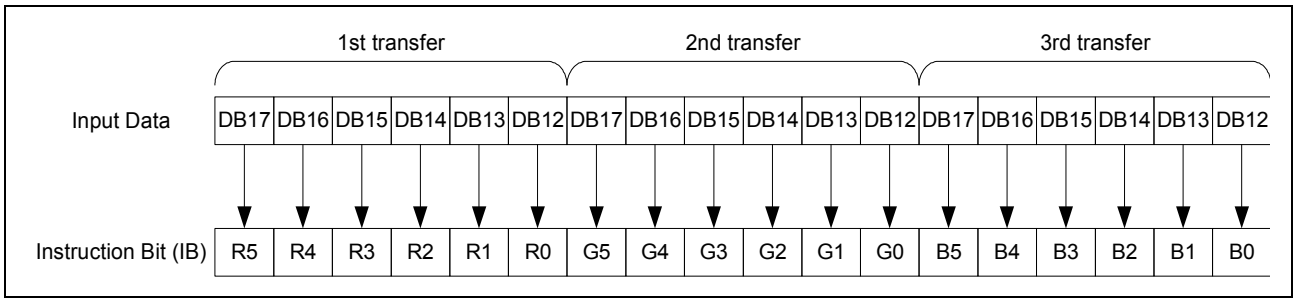


Figure 18. 260k color data transfer on 8-bit parallel bus (MDT = 2'b10)

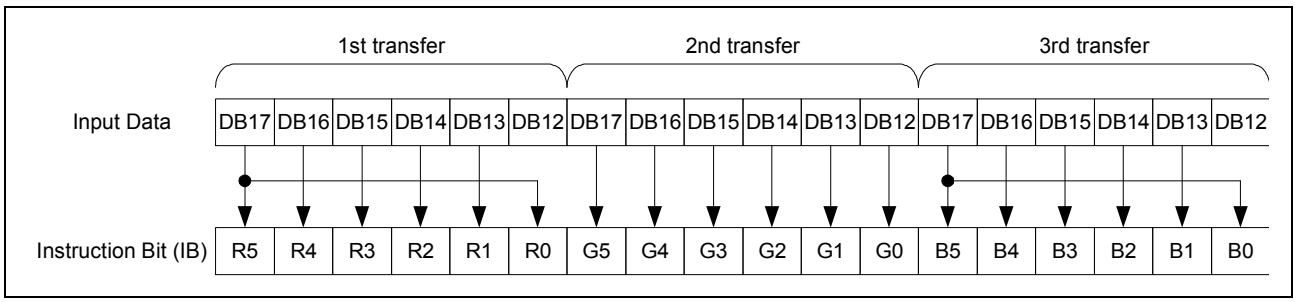


Figure 19. 65k color data transfer on 8-bit parallel bus by 3-times data transfer (MDT = 2'b11)

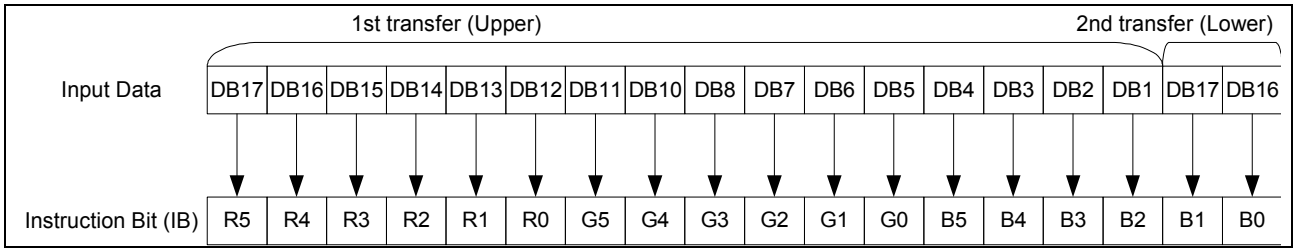


Figure 20. 260k color data transfer on 16-bit parallel bus (MDT = 2'b10)

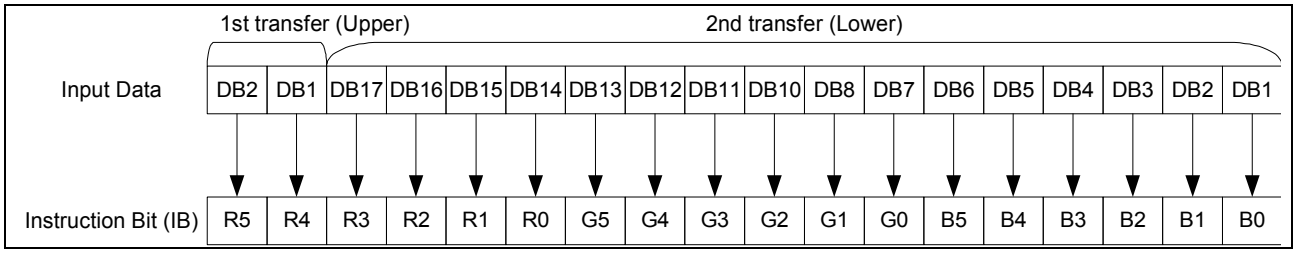


Figure 21. 260k color data transfer on 16-bit parallel bus (MDT = 2'b11).

ID

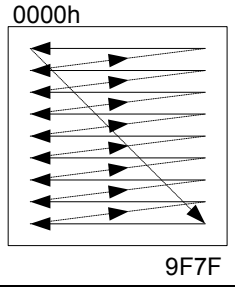
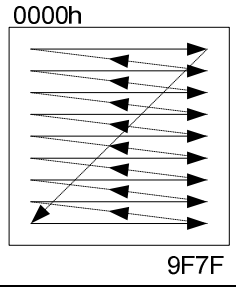
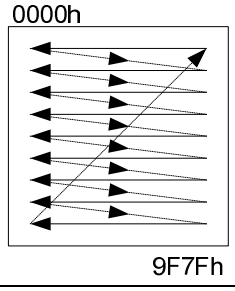
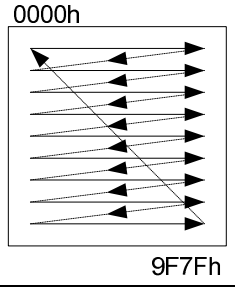
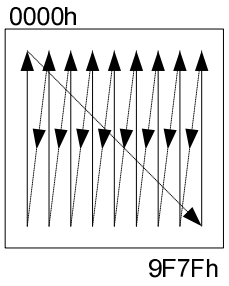
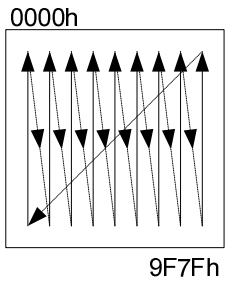
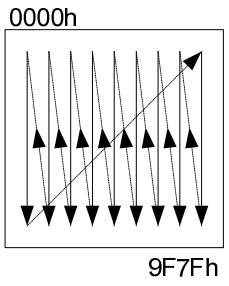
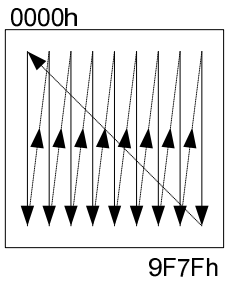
When ID[1], ID[0] = 1, the address counter (AC) is automatically increased by 1 after the data is written to the GRAM. When ID[1], ID[0] = 0, the AC is automatically decreased by 1 after the data is written to the GRAM.

The increment/decrement setting of the address counter using ID[1:0] is done independently of the horizontal and vertical addresses.

AM

Sets the automatic update method of the AC after the data is written to GRAM. When AM = 0, the data is continuously written in horizontally. When AM = 1, the data is continuously written vertically. When window addresses are specified, the GRAM in the window range can be written according to the ID[1:0] and AM settings.

Table 27. Address Direction Setting

	ID[1:0] = 00 H: decrement V: decrement	ID[1:0] = 01 H: increment V: decrement	ID[1:0] = 10 H: decrement V: increment	ID[1:0] = 11 H: increment V: increment
AM=0 Horizontal Update				
AM=1 Vertical Update				

[Note]

When window addresses have been set, the GRAM can only be written within the window.

When AM is '1', abnormal display can appear on screen.

When AM or ID is set, start address should be written accordingly prior to memory write.

8.3.7. Display control (R07h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	X	X	X	PT1	PT0	X	X	SPT	X	X	GON	DTE	CL	REV	D1	D0

PT

Normalizes the source outputs when non-displayed area of the partial display is driven. For details, refer to Screen-division Driving Function section. Note that the control with PT is not affected by REV.

Table 28. Non-Displayed Area Control

CL	PT[1:0]	Source Output for Non-display Area		Gate Output for Non-display Area
		Positive Polarity	Negative Polarity	
0	00	V63	V0	Normal Drive
	01	V0	V63	Normal Drive
	10	GND	GND	VGL
	11	Hi-z	Hi-z	VGL
1	00	VSSA	GVDD	Normal Drive
	01	GVDD	VSSA	Normal Drive
	10	GND	GND	VGL
	11	Hi-z	Hi-z	VGL

[Note] In this table, GND means source driver's outputs are short to VcomOUT level.

SPT

When SPT = 1, the Split Screen Driving Function is performed. This function is not available when RGB interface is in use. For details, refer to Split Screen Driving Function section which will be described later.

GON / DTE

GON and DTE set gate output (G1 to G160) according to the settings shown in Table 29.

Table 29. Gate Clock Control.

GON	DTE	Gate output	VCOMOUT
0	X	VGH	Halt (VSS)
1	0	VGL	Normal operation
	1	VGH/VGL	Normal operation

CL

CL = 1 selects 8-color display mode. For details, refer to 8-color Display Mode section.

Table 30. Color Depth Control.

CL	Color Depth
0	262,144 colors / 65,536 colors
1	8 colors

REV

Displays all character and graphics display sections with reversal when REV = 1. Since the grayscale level can be reversed, display of the same data can be enabled normally for both white and black panels.

Table 31. Source Output Control in operation.

REV	GRAM data	Source output level									
		Display Area		Non-display area							
				PT[1:0] = 00		PT[1:0] = 01		PT[1:0] = 10		PT[1:0] = 11	
		Positive	Negative	Positive	Negative	Positive	Negative	Positive	Negative	Positive	Negative
0	6'b000000 : 6'h111111	V63 : V0	V0 : V63	V63	0	V0	V63	VSS	VSS	Hi-z	Hi-z
1	6'b000000 : 6'h111111	V0 : V63	V63 : V0								

D

Display is on when D[1] = 1 and off when D[1] = 0. When off, the display data remains in the GRAM, and can be re-displayed instantly by setting D[1] = 1. When D[1] is 0, the display is off with the entire source outputs set to the VSS level. Because of this, the S6D0151 can control the charging current for the LCD with AC driving. The display can be turned on or off with GON and DTE bits. For details, refer to Instruction Set-up Flow section.

When D[1:0] = 01, the internal display of the S6D0151 is performed although the display is off. When D[1:0] = 00, the internal display operation halts and the display is off.

Table 32. Source Output Control

D[1:0]	GON	DTE	Source	VCOM	Gate	Display
00	0	X	VSS	VSS	VGH	White On normally white Panel Black On normally Black Panel
00	1	0	VSS	VSS	VGL	-
00	1	1	Not available			
01	0	X	VSS	VSS	VGH	White On normally white Panel Black On normally Black Panel
01	1	0	VSS	VSS	VGL	-
01	1	1			VGH/VGL	White On normally white Panel Black On normally Black Panel
10	0	X	Not available			
10	1	0	GVDD/ VSS	VCOMH/ VCOML	VGL	-
10	1	1			VGH/VGL	White On normally white Panel Black On normally Black Panel
11	0	X	Not available			
11	1	0	Data	VCOMH/ VCOML	VGL	-
11	1	1			VGH/VGL	RAM data

[Note]

1. Writing from MCU to GRAM is independent from D.
2. In sleep and standby modes, S6D0151 operates as if D[1:0] = 00. The register of D is not modified.
3. In this table, GND means source driver's outputs are shorted to the VcomOUT level.

8.3.8. Blank period control 1 (R08h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	X	X	X	X	FP3	FP2	FP1	FP0	X	X	X	X	BP3	BP2	BP1	BP0

FP/BP

Sets the period of blank period, which is placed at the beginning and the end of a frame. FP[3:0] is for a Front Porch and BP[3:0] is for a Back Porch. When Front and Back porches are set, the following conditions are satisfied

BP+FP ≤16 lines

FP ≥2 lines

BP ≥2 lines

When the S6D0151 operates in the external clock operation mode, Back Porch (BP) will start on the falling edge of the VSYNC signal and display operation begins just after the back porch period. Front Porch (FP) will start when the data of number of lines specified by NL has been displayed. During the period between the completion of front porch and the next VSYNC signal, the display will remain blank.

Table 33. Blank Period Control with FP and BP.

FP[3:0] (BP[3:0])	Number of Raster Periods In Front (Back) Porch
0000	Not available
0001	Not available
0010	2
0011	3
0100	4
---	---
1000	8
---	---
1100	12
1101	13
1110	14
1111	Not available

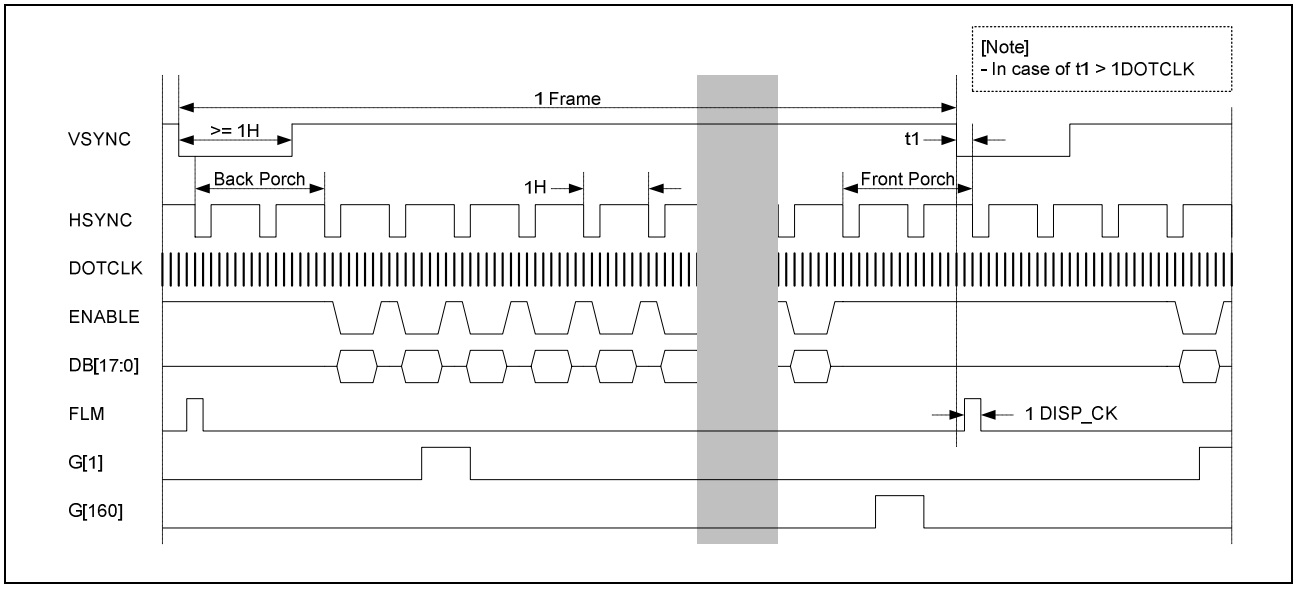


Figure 22. BP & FP in external clock operation mode (DM[0] = 1).

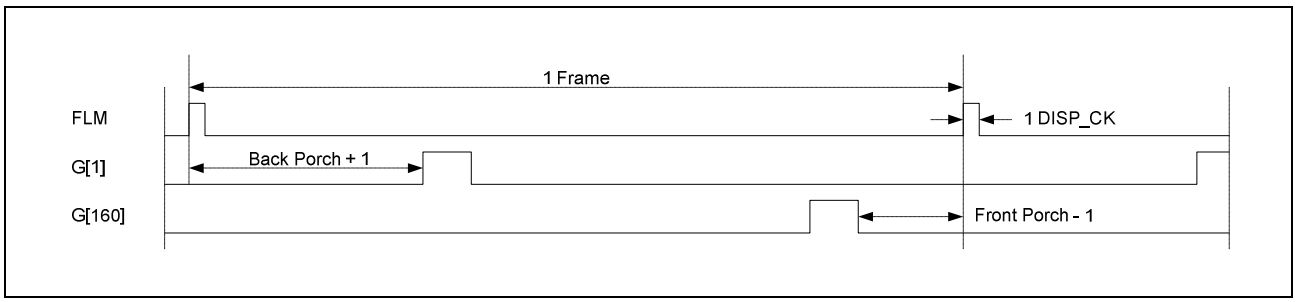


Figure 23. BP & FP in internal clock operation mode (DM[0] = 0).

[Note] DISP_CK : OSCK_CK divided by DIV[1:0](DM = 2'b00) or DOTCLK divided by 8(DM = 2'b01 and RIM[1] = 1'b1)

8.3.9. Frame cycle control (R0Bh)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	X	X	X	X	X	X	DIV 1	DIV 0	X	X	X	X	RTN 3	RTN 2	RTN 1	RTN 0

DIV

Sets the division ratio of clocks for internal operation. Internal operations are driven by clocks, which are frequency divided according to the value of this register. Frame frequency can be adjusted with this. When changing the number of the drive cycle, adjust the frame frequency.

Table 34. Frame Frequency Control.

DIV[1:0]	Division Ratio	Internal operation clock frequency
00	1	fosc/1
01	2	fosc/2
10	4	fosc/4
11	8	fosc/8

[Note] fosc = R-C oscillation frequency. The clock is divided by DIV is defined as INCLK

$$\text{Frame Frequency} = \frac{f_{osc}}{\text{Clock cycles per raster-row x division ratio x (Line+B)}} \text{ [Hz]}$$

f_{osc}: R-C oscillation frequency
Line: Number of raster-rows (NL bit)
Clock cycles per raster-row: RTN bit
Division ratio: DIV bit
B: Blank period(Back porch + Front Porch)

Figure 24. Formula for the frame frequency.

RTN

Sets the 1H period.

Table 35. Clock Cycles per horizontal line.

RTN[3:0]	Clock Cycles per horizontal Line
0000	16 (INCLKs)
0001	17 (INCLKs)
---	---
1110	30 (INCLKs)
1111	31 (INCLKs)

8.3.10. External Display Interface Control (R0Ch)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	X	X	X	X	X	X	X	RM	X	X	DM1	DM0	X	X	RIM 1	RIM 0

RM

The interface for GRAM access can be set according to Table 36. This register and DM register can be set independently. The display data can be written through system interface by clearing this register even though the RGB interface is being used.

Table 36. RM and GRAM Access Interface.

RM	GRAM Access Interface
0	System interface
1	RGB interface

DM

Specifies the display operation mode. The interface can be set according to the bits of DM[1:0]. In the Internal Clock Operation mode source clock for display operation comes from internal oscillator while in the External Clock Operation mode it comes from RGB interface (DOTCLK, VSYNC, HSYNC).

Table 37. DM and Display Operation Modes.

DM[1:0]	Display operation mode
00	Internal clock operation
01	External clock operation
10	Reserved
11	Reserved

RIM

Specifies the RGB interface mode when the RGB interface is used. This register is valid when RM is set to 1. DM and this register should be set before proper display operation is performed through the RGB interface.

Table 38. RIM and RGB Interface Modes.

RIM[1:0]	RGB Interface mode
00	6-bit RGB interface (three transfers per pixel)
01	16-bit RGB interface (one transfer per pixel)
10	18-bit RGB interface (one transfer per pixel)
11	Reserved

8.3.11. Power Control 1 (R10h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	X	X	SAP2	SAP1	SAP0	BT2	BT1	BT0	DC2	DC1	DC0	AP2	AP1	AP0	SLP	STB

SAP

Adjusts the slew-rate of the operational amplifier for the source driver. If higher SAP2-0 is set, LCD panel having higher resolution or higher frame frequency can be driven because the slew-rate of the operational amplifier is increased. But, these bits must be set carefully since the currents consumed in the operational amplifiers vary accordingly. During non-display, when SAP2-0 = 000, the lowest current consumption level is attained.

Table 39. Current and Slew Rate Control.

SAP[2:0]	Slew-Rate of Operational Amplifier	Amount of Current in Operational Amplifier
000	Operation of the operational amplifier halted.	
001	Not available	Not available
010	Slow or medium	Small or medium
011	Medium	Medium
100	Medium or fast	Medium or large
101	Fast	Large
110	Not available	Not available
111	Not available	Not available

BT

The output adjust scale factor of the DC/DC converter2 circuit is selected.

Table 40. Multiplication scale factor selection of DC/DC converter2.

BT[2:0]	VGH Output	VGL Output	Notes
000	AVDD X 3	-(AVDDx2+VCI1)	VGH = Vci1 X six times
001		-(AVDDx2)	VGH = Vci1 X six times
010		-(AVDD+VCI1)	VGH = Vci1 X six times
011	AVDD X 2 + VCI1	-(AVDDx2+VCI1)	VGH = Vci1 X five times
100		-(AVDDx2)	VGH = Vci1 X five times
101		-(AVDD+VCI1)	VGH = Vci1 X five times
110	AVDD X 2	-(AVDDx2)	VGH = Vci1 X four times
111		-(AVDD+VCI1)	VGH = Vci1 X four times

DC

The operating frequency of the DC/DC converters is selected. When the DC/DC converter operating frequency is high, the driving ability of the DC/DC converter and the display quality become high, but they come at a cost of higher current consumption. The final value of the frequency should be determined through performance tradeoffs between the display quality and the overall current consumption level. Valid settings for R69h NLPM=0 are shown below in Table 41.

Table 41. Frequency scale factor.

DC[2:0]	DC/DC Converter Cycle	
	DC/DC Converter1/2	DC/DC Converter2
000	DCCLK / 1	DCCLK / 2
001	DCCLK / 2	DCCLK / 2
010	DCCLK / 4	DCCLK / 2
011	DCCLK / 2	DCCLK / 8
100	DCCLK / 1	DCCLK / 4
101	DCCLK / 2	DCCLK / 4
110	DCCLK / 4	DCCLK / 4
111	DCCLK / 4	DCCLK / 8

AP

The level of static current in the operational amplifier for the power supply can be altered. When the static current level is large, the LCD driving ability and the display quality is relatively high, but so is the current consumption level. The final value of the static current level should be determined through performance tradeoff between the display quality and the overall current consumption level. During no display mode (AP2-0 = 000), the overall current consumption can be reduced by terminating the operational amplifier and the DC/DC converter circuitry operations. If AP2-0 ≠ 000, the DC/DC converter circuitry is in operation. For further information about timing, refer to Set-up Flow of Power Supply Circuit and Timing Diagram of Power setting sections.

Table 42. Current Control.

AP[2:0]	Amount of Current in Operational Amplifier	DC/DC converter operation
000	Operation of the operational amplifier stops.	Halt
001	Small	Operate (VCI1, AVDD, VGH, VGL, VCL)
010	Small or medium	
011	Medium	
100	Medium or large	
101	Large	
110	Not available	
111	Not available	

SLP

When SLP = 1, the S6D0151 enters the sleep mode, where the internal display operations are halted except for the R-C oscillator, thus reducing current consumption. Only the following instructions can be executed during the sleep mode.

- Power control (BT2–0, DC3–0, AP2–0, SLP, STB, VRH5-0, VCOMG, VDV6-0, and VCM6-0 bits)

In the sleep mode, other GRAM data and instructions cannot be updated although their values are retained while G1 to G160 outputs are tied to the VSS voltage level, and register set-up is protected (maintained).

STB

When STB = 1, the S6D0151 enters the standby mode, where display operation completely stops, halting all internal operations including the internal R-C oscillator. Further, no external clock pulses are supplied. For details, refer to Sequence of Standby/Sleep Mode section. Only the following instructions can be executed during the standby mode.

- Standby mode cancel (STB = 0)
- Start oscillation

Table 43. Operation Mode Summary.

Mode	Operation	Oscillator	RVDD
Normal	Active	Active	Active
Sleep	Inactive	Active	Active
Standby	Inactive	Inactive	Active

8.3.12. Gamma control 1 (R11h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	VR1C	X	X	VRN14	VRN13	VRN12	VRN11	VRN10	X	X	X	VRP14	VRP13	VRP12	VRP11	VRP10

VR1C

Controls the step amplitude of positive and negative 64-grayscales. For details, refer to Gamma Adjustment Function section.

VRP1[4:0]

Controls the amplitude of positive 64-grayscale. For details, refer to Gamma Adjustment Function section.

VRN1[4:0]

Controls the amplitude of negative 64-grayscale. For details, refer to Gamma Adjustment Function section.

8.3.13. Power control 2 (R12h)

8.3.14. Power control 3 (R13h)

8.3.15. Power control 4 (R14h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	X	X	X	X	X	X	X	X	SVC 3	SVC 2	SVC 1	SVC 0	X	0	VRH 5	VRH 4
W	1	X	X	X	X	VC MR	X	X	X	X	X	X	PON	VRH 3	VRH 2	VRH 1	VRH 0
W	1	X	VDV 6	VDV 5	VDV 4	VDV 3	VDV 2	VDV 1	VDV 0	VCO MG	VC M6	VC M5	VC M4	VC M3	VC M2	VC M1	VC M0

SVC

Adjusts the reference voltages of AVDD, VGH, VGL and VCL

Table 44. VCI1 voltage setting.

SVC[3:0]	VCI1 [Without Load]
0000	2.10 V
0001	2.16 V
0010	2.22 V
0011	2.28 V
0100	2.34 V
0101	2.40 V
0110	2.46 V
0111	2.52 V
1000	2.58 V
1001	2.64 V
1010	2.70 V
1011	2.76 V
1100	Not available
1101	Not available
1110	Not available
1111	Not available

[Note] VCI = VCI1, when VCI is lower than VCI1.

PON

This bit controls the on/off states of the integrated amplifiers. PON = 0 stops and PON = 1 starts the IC operation. For further information about timing, refer to Set-up Flow of Power Supply Circuit and Timing Diagram of Power setting sections..

VCMR

Selects the method for VCOMH adjustment. This can be done through external resistor setting (VCOMR) or internal voltage divider setting (VCM) bits.

Table 45. VCOMH Control.

VCMR	VCOMH voltage
0	VCOMR
1	Internal voltage divider

VRH5-0

Sets the maximum upper side voltage for the gamma (GVDD) block. GVDD voltage is directly generated from power reference value, VCIR_EXIN (tied to 2.0V); The GVDD voltage ranges from 3.0 to 5.0V

Table 46. GVDD setting.

VRH[5:0]	GVDD Output	VRH[5:0]	GVDD Output
000000	VCIR_EXIN X 1.500 = 3.00V	010110	VCIR_EXIN X 2.050 = 4.10V
000001	VCIR_EXIN X 1.525 = 3.05V	010111	VCIR_EXIN X 2.075 = 4.15V
000010	VCIR_EXIN X 1.550 = 3.10V	011000	VCIR_EXIN X 2.100 = 4.20V
000011	VCIR_EXIN X 1.575 = 3.15V	011001	VCIR_EXIN X 2.125 = 4.25V
000100	VCIR_EXIN X 1.600 = 3.20V	011010	VCIR_EXIN X 2.150 = 4.30V
000101	VCIR_EXIN X 1.625 = 3.25V	011011	VCIR_EXIN X 2.175 = 4.35V
000110	VCIR_EXIN X 1.650 = 3.30V	011100	VCIR_EXIN X 2.200 = 4.40V
000111	VCIR_EXIN X 1.675 = 3.35V	011101	VCIR_EXIN X 2.225 = 4.45V
001000	VCIR_EXIN X 1.700 = 3.40V	011110	VCIR_EXIN X 2.250 = 4.50V
001001	VCIR_EXIN X 1.725 = 3.45V	011111	VCIR_EXIN X 2.275 = 4.55V
001010	VCIR_EXIN X 1.750 = 3.50V	100000	VCIR_EXIN X 2.300 = 4.60V
001011	VCIR_EXIN X 1.775 = 3.55V	100001	VCIR_EXIN X 2.325 = 4.65V
001100	VCIR_EXIN X 1.800 = 3.60V	100010	VCIR_EXIN X 2.350 = 4.70V
001101	VCIR_EXIN X 1.825 = 3.65V	100011	VCIR_EXIN X 2.375 = 4.75V
001110	VCIR_EXIN X 1.850 = 3.70V	100100	VCIR_EXIN X 2.400 = 4.80V
001111	VCIR_EXIN X 1.875 = 3.75V	100101	VCIR_EXIN X 2.425 = 4.85V
010000	VCIR_EXIN X 1.900 = 3.80V	100110	VCIR_EXIN X 2.450 = 4.90V
010001	VCIR_EXIN X 1.925 = 3.85V	100111	VCIR_EXIN X 2.475 = 4.95V
010010	VCIR_EXIN X 1.950 = 3.90V	101000	VCIR_EXIN X 2.500 = 5.00V
010011	VCIR_EXIN X 1.975 = 3.95V	101001	Not available
010100	VCIR_EXIN X 2.000 = 4.00V	:	:
010101	VCIR_EXIN X 2.025 = 4.05V	111111	Not available

[Note]

1. VRH5-0 setting value is limited to GVDD output is no more than (AVDD-0.3)

2. GVDD = 3 + (0.05 * VRH)

VCOMG

When VCOMG = 1, VcomL can output negative voltage. When VCOMG = 0, VcomL voltage settles to VSS voltage and stops the amplifier from generating negative voltage; this behavior lead to lower power consumption. When VCOMG = 0 and Vcom is AC driven, VDV6-0 bits became don't cares. In this case, Vcom A/C amplitude can only be adjusted per VCM6-0 bits.

VDV

Sets the amplitude of VCOM signal. It can be chosen from the range of 0.540 ~ 1.2 times the voltage of GVDD. When Vcom signal does not toggle, i.e., not driven, the settings become invalid.

Table 47. Vcom Amplitude Control.

VDV[6:0]	Vcom Amplitude	VDV[6:0]	Vcom Amplitude	VDV[6:0]	Vcom Amplitude
0000000	Not available	0110100	GVDD x 0.750	1011010	GVDD x 0.978
:	Not available	0110101	GVDD x 0.756	1011011	GVDD x 0.984
0010000	Not available	0110110	GVDD x 0.762	1011100	GVDD x 0.990
0010001	GVDD x 0.540	0110111	GVDD x 0.768	1011101	GVDD x 0.996
0010010	GVDD x 0.546	0111000	GVDD x 0.774	1011110	GVDD x 1.002
0010011	GVDD x 0.552	0111001	GVDD x 0.780	1011111	GVDD x 1.008
0010100	GVDD x 0.558	0111010	GVDD x 0.786	1100000	GVDD x 1.014
0010101	GVDD x 0.564	0111011	GVDD x 0.792	1100001	GVDD x 1.020
0010110	GVDD x 0.570	0111100	GVDD x 0.798	1100010	GVDD x 1.026
0010111	GVDD x 0.576	0111101	GVDD x 0.804	1100011	GVDD x 1.032
0011000	GVDD x 0.582	0111110	GVDD x 0.810	1100100	GVDD x 1.038
0011001	GVDD x 0.588	0111111	GVDD x 0.816	1100101	GVDD x 1.044
0011010	GVDD x 0.594	1000000	GVDD x 0.822	1100110	GVDD x 1.050
0011011	GVDD x 0.600	1000001	GVDD x 0.828	1100111	GVDD x 1.056
0011100	GVDD x 0.606	1000010	GVDD x 0.834	1101000	GVDD x 1.062
0011101	GVDD x 0.612	1000011	GVDD x 0.840	1101001	GVDD x 1.068
0011110	GVDD x 0.618	1000100	GVDD x 0.846	1101010	GVDD x 1.074
0011111	GVDD x 0.624	1000101	GVDD x 0.852	1101011	GVDD x 1.080
0100000	GVDD x 0.630	1000110	GVDD x 0.858	1101100	GVDD x 1.086
0100001	GVDD x 0.636	1000111	GVDD x 0.864	1101101	GVDD x 1.092
0100010	GVDD x 0.642	1001000	GVDD x 0.870	1101110	GVDD x 1.098
0100011	GVDD x 0.648	1001001	GVDD x 0.876	1101111	GVDD x 1.104
0100100	GVDD x 0.654	1001010	GVDD x 0.882	1110000	GVDD x 1.110
0100101	GVDD x 0.660	1001011	GVDD x 0.888	1110001	GVDD x 1.116
0100110	GVDD x 0.666	1001100	GVDD x 0.894	1110010	GVDD x 1.122
0100111	GVDD x 0.672	1001101	GVDD x 0.900	1110011	GVDD x 1.128
0101000	GVDD x 0.678	1001110	GVDD x 0.906	1110100	GVDD x 1.134
0101001	GVDD x 0.684	1001111	GVDD x 0.912	1110101	GVDD x 1.140
0101010	GVDD x 0.690	1010000	GVDD x 0.918	1110110	GVDD x 1.146
0101011	GVDD x 0.696	1010001	GVDD x 0.924	1110111	GVDD x 1.152
0101100	GVDD x 0.702	1010010	GVDD x 0.930	1111000	GVDD x 1.158
0101101	GVDD x 0.708	1010011	GVDD x 0.936	1111001	GVDD x 1.164
0101110	GVDD x 0.714	1010100	GVDD x 0.942	1111010	GVDD x 1.170
0101111	GVDD x 0.720	1010101	GVDD x 0.948	1111011	GVDD x 1.176
0110000	GVDD x 0.726	1010110	GVDD x 0.954	1111100	GVDD x 1.182
0110001	GVDD x 0.732	1010111	GVDD x 0.960	1111101	GVDD x 1.188
0110010	GVDD x 0.738	1011000	GVDD x 0.966	1111110	GVDD x 1.194
0110011	GVDD x 0.744	1011001	GVDD x 0.972	1111111	GVDD x 1.200

[Note]

Adjust the register VRH5-0 and VDV6-0 so that the Vcom amplitude is lower than 6.0 V.

VcomL voltage should be : VCL+0.5 < VcomL <0.0V

VCM

Sets VcomH voltage, which is equal to the maximum voltage Vcom signal reaches as it is being toggled. VCM bits determine the voltage of VcomH in accordance with Table 48. The voltage can be chosen from the range of 0.4015 ~ 1.1 times that of GVDD voltage. However, there is a precondition that must be satisfied before VCM bits can choose the VcomH voltage; MTP_SEL bit and VCMR bits must be set to 0 and 1, respectively. If MTP_SEL bit has been set to 1, then the voltage of VcomH would be determined by the stored data of MTP. On the other hand, if VCMR bit has been set to 0, then the voltage would be determined by an external resistor connected to VCOMR pad.

Table 48. VcomH Control.

VCM[6:0]	VcomH Voltage	VCM[6:0]	VcomH Voltage	VCM[6:0]	VcomH Voltage
0000000	GVDD x 0.4015	0101011	GVDD x 0.6380	1010110	GVDD x 0.8745
0000001	GVDD x 0.4070	0101100	GVDD x 0.6435	1010111	GVDD x 0.8800
0000010	GVDD x 0.4125	0101101	GVDD x 0.6490	1011000	GVDD x 0.8855
0000011	GVDD x 0.4180	0101110	GVDD x 0.6545	1011001	GVDD x 0.8910
0000100	GVDD x 0.4235	0101111	GVDD x 0.6600	1011010	GVDD x 0.8965
0000101	GVDD x 0.4290	0110000	GVDD x 0.6655	1011011	GVDD x 0.9020
0000110	GVDD x 0.4345	0110001	GVDD x 0.6710	1011100	GVDD x 0.9075
0000111	GVDD x 0.4400	0110010	GVDD x 0.6765	1011101	GVDD x 0.9130
0001000	GVDD x 0.4455	0110011	GVDD x 0.6820	1011110	GVDD x 0.9185
0001001	GVDD x 0.4510	0110100	GVDD x 0.6875	1011111	GVDD x 0.9240
0001010	GVDD x 0.4565	0110101	GVDD x 0.6930	1100000	GVDD x 0.9295
0001011	GVDD x 0.4620	0110110	GVDD x 0.6985	1100001	GVDD x 0.9350
0001100	GVDD x 0.4675	0110111	GVDD x 0.7040	1100010	GVDD x 0.9405
0001101	GVDD x 0.4730	0111000	GVDD x 0.7095	1100011	GVDD x 0.9460
0001110	GVDD x 0.4785	0111001	GVDD x 0.7150	1100100	GVDD x 0.9515
0001111	GVDD x 0.4840	0111010	GVDD x 0.7205	1100101	GVDD x 0.9570
0010000	GVDD x 0.4895	0111011	GVDD x 0.7260	1100110	GVDD x 0.9625
0010001	GVDD x 0.4950	0111100	GVDD x 0.7315	1100111	GVDD x 0.9680
0010010	GVDD x 0.5005	0111101	GVDD x 0.7370	1101000	GVDD x 0.9735
0010011	GVDD x 0.5060	0111110	GVDD x 0.7425	1101001	GVDD x 0.9790
0010100	GVDD x 0.5115	0111111	GVDD x 0.7480	1101010	GVDD x 0.9845
0010101	GVDD x 0.5170	1000000	GVDD x 0.7535	1101011	GVDD x 0.9900
0010110	GVDD x 0.5225	1000001	GVDD x 0.7590	1101100	GVDD x 0.9955
0010111	GVDD x 0.5280	1000010	GVDD x 0.7645	1101101	GVDD x 1.0010
0011000	GVDD x 0.5335	1000011	GVDD x 0.7700	1101110	GVDD x 1.0065
0011001	GVDD x 0.5390	1000100	GVDD x 0.7755	1101111	GVDD x 1.0120
0011010	GVDD x 0.5445	1000101	GVDD x 0.7810	1110000	GVDD x 1.0175
0011011	GVDD x 0.5500	1000110	GVDD x 0.7865	1110001	GVDD x 1.0230
0011100	GVDD x 0.5555	1000111	GVDD x 0.7920	1110010	GVDD x 1.0285
0011101	GVDD x 0.5610	1001000	GVDD x 0.7975	1110011	GVDD x 1.0340
0011110	GVDD x 0.5665	1001001	GVDD x 0.8030	1110100	GVDD x 1.0395
0011111	GVDD x 0.5720	1001010	GVDD x 0.8085	1110101	GVDD x 1.0450
0100000	GVDD x 0.5775	1001011	GVDD x 0.8140	1110110	GVDD x 1.0505
0100001	GVDD x 0.5830	1001100	GVDD x 0.8195	1110111	GVDD x 1.0560
0100010	GVDD x 0.5885	1001101	GVDD x 0.8250	1111000	GVDD x 1.0615
0100011	GVDD x 0.5940	1001110	GVDD x 0.8305	1111001	GVDD x 1.0670
0100100	GVDD x 0.5995	1001111	GVDD x 0.8360	1111010	GVDD x 1.0725
0100101	GVDD x 0.6050	1010000	GVDD x 0.8415	1111011	GVDD x 1.0780
0100110	GVDD x 0.6105	1010001	GVDD x 0.8470	1111100	GVDD x 1.0835
0100111	GVDD x 0.6160	1010010	GVDD x 0.8525	1111101	GVDD x 1.0890
0101000	GVDD x 0.6215	1010011	GVDD x 0.8580	1111110	GVDD x 1.0945
0101001	GVDD x 0.6270	1010100	GVDD x 0.8635	1111111	GVDD x 1.1000
0101010	GVDD x 0.6325	1010101	GVDD x 0.8690	-	-

8.3.16. GRAM address set (R21h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	AD 15	AD 14	AD 13	AD 12	AD 11	AD 10	AD 9	AD 8	AD 7	AD 6	AD 5	AD 4	AD 3	AD 2	AD 1	AD 0

AD

Address Counter (AC) can be loaded with initial GRAM address. When GRAM data is transferred through System Interface or RGB Interface, the AC is automatically updated according to AM and ID registers. This allows consecutive writes without re-setting the address in AC. But when GRAM data is read, the AC is not automatically updated.

GRAM address setting is not allowed in Standby mode. Ensure that the address is set within the specified window area described by VSA, VEA, HSA and HEA registers.

When RGB interface is used (RM=1) to access GRAM, AD[16:0] will set the address counter at the falling edge of the VSYNC signal. And when System Interface is used to access GRAM (RM = 0), AD[16:0] will be set.

Table 49. GRAM Address Range.

AD[15:0]	GRAM setting
0000h to 007Fh	Bitmap data for G1
0100h to 017Fh	Bitmap data for G2
0200h to 027Fh	Bitmap data for G3
0300h to 037Fh	Bitmap data for G4
: : :	: : :
9C00h to 9C7Fh	Bitmap data for G157
9D00h to 9D7Fh	Bitmap data for G158
9E00h to 9E7Fh	Bitmap data for G159
9F00h to 9F7Fh	Bitmap data for G160

8.3.17. Write Data to GRAM (R22h)

R/W	RS	
W	1	RAM write data (WD17 ~ WB0). *Interface mode controls the width of WD

WDR

All data being loaded onto DB bus will comply with its 18-bit bus-width. The loaded data, then, will be written to GRAM and eventually outputted by the IC's source drivers. Keep in mind that the expansion format varies with interface mode. GRAM cannot be accessed in Standby mode. When data is written to GRAM via system interface while another data is being written through RGB interface, make sure that the two write operations are not in conflict. A flow chart describing memory-data-write sequences is shown in Figure 25.

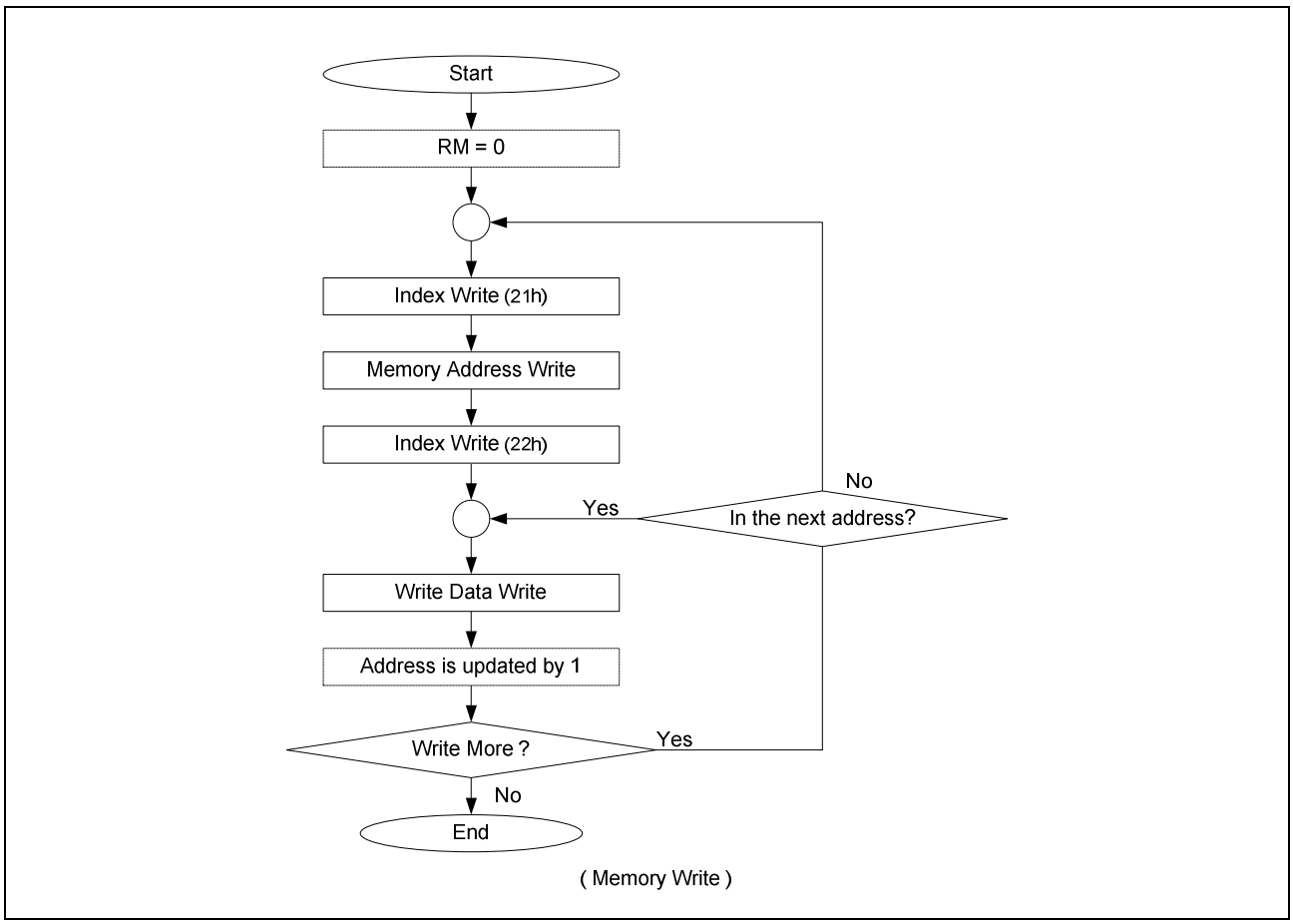


Figure 25. Memory data write sequence.

8.3.18. Read data from GRAM (R22h)

RDR

Data can be read from GRAM through this register. When you make read operations, you can get a proper data on the second read operation as shown below. A flow chart describing memory-data-read sequences is shown in Figure 26. Note that the valid data appears on a second read operation, which always should be proceeded by a dummy read operation.

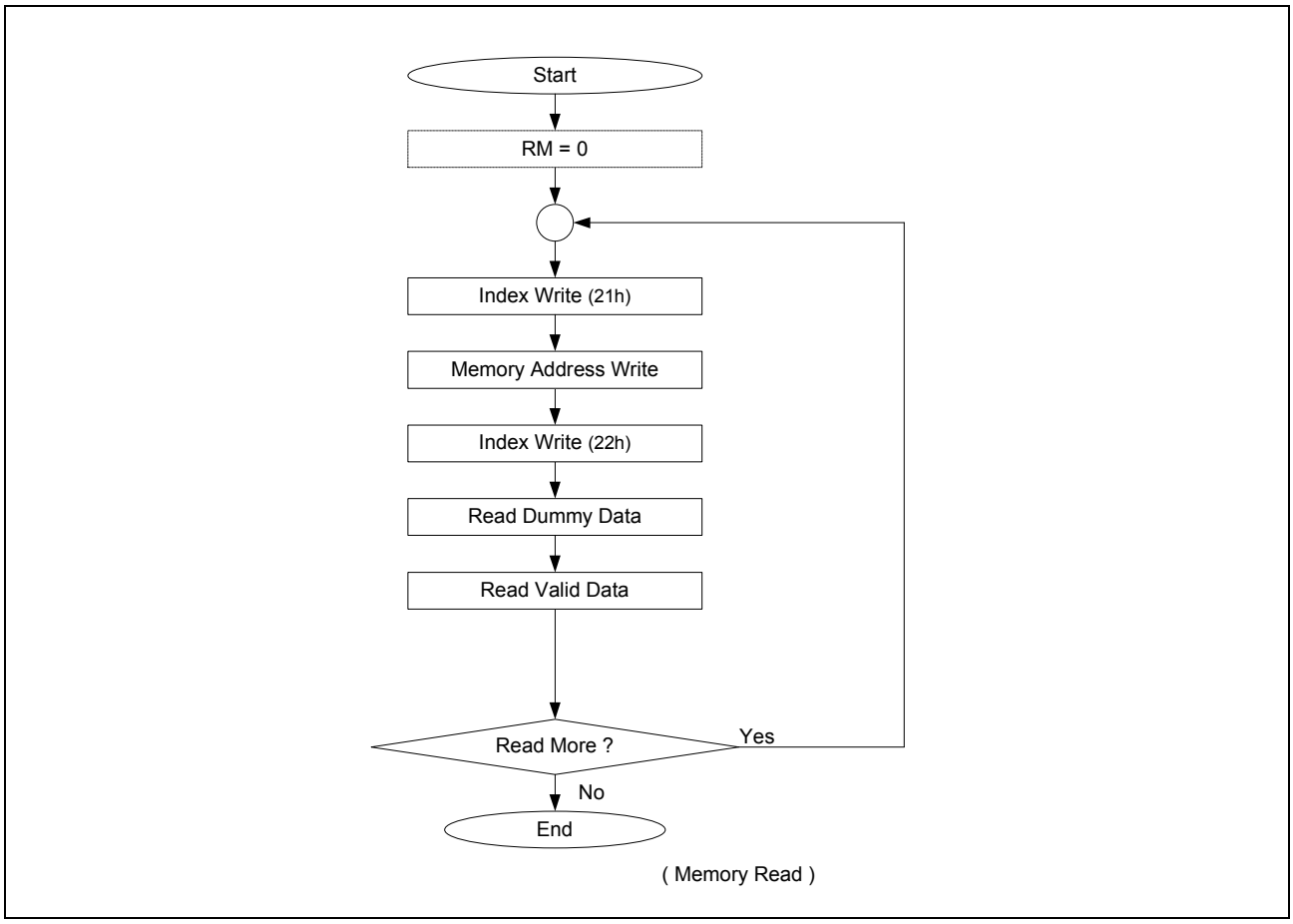


Figure 26. Memory data read sequence

8.3.19. Gamma control 2 (R30h to R37h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	X	X	X	X	X	PKP 12	PKP 11	PKP 10	X	X	X	X	X	PKP 02	PKP 01	PKP 00
W	1	X	X	X	X	X	PKP 32	PKP 31	PKP 30	X	X	X	X	X	PKP 22	PKP 21	PKP 20
W	1	X	X	X	X	X	PKP 52	PKP 51	PKP 50	X	X	X	X	X	PKP 42	PKP 41	PKP 40
W	1	X	X	X	X	X	PRP 12	PRP 11	PRP 10	X	X	X	X	X	PRP 02	PRP 01	PRP 00
W	1	X	X	X	X	X	PKN 12	PKN 11	PKN 10	X	X	X	X	X	PKN 02	PKN 01	PKN 00
W	1	X	X	X	X	X	PKN 32	PKN 31	PKN 30	X	X	X	X	X	PKN 22	PKN 21	PKN 20
W	1	X	X	X	X	X	PKN 52	PKN 51	PKN 50	X	X	X	X	X	PKN 42	PKN 41	PKN 40
W	1	X	X	X	X	X	PRN 12	PRN 11	PRN 10	X	X	X	X	X	PRN 02	PRN 01	PRN 00

PKP5[2:0], PKP4[2:0], PKP3[2:0], PKP2[2:0], PKP1[2:0], PKP0[2:0]

The gamma fine adjustment registers for the positive polarity output are shown

PRP1[2:0], PRP0[2:0]

The gradient adjustment registers for the positive polarity output are shown

PKN5[2:0], PKN4[2:0], PKN3[2:0], PKN2[2:0], PKN1[2:0], PKN0[2:0]

The gamma fine adjustment registers for the negative polarity output are shown

PRN1[2:0], PRN0[2:0]

The gradient adjustment registers for the negative polarity output are shown
For details, see Gamma Adjustment Function section.

8.3.20. Gamma control 3 (R38h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	X	X	X	X	VRN 03	VRN 02	VRN 01	VRN 00	X	X	X	X	VRP 03	VRP 02	VRP 01	VRP 00

VRP0[3:0]

Controls amplitude positive polarity of 64-grayscale. For details, refer to Gamma Adjustment Function section.

VRN0[3:0]

Controls amplitude negative polarity of 64-grayscale. For details, refer to Gamma Adjustment Function section.

8.3.21. Gate scan position (R40h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	X	X	X	X	X	X	X	X	X	X	X	SCN 4	SCN 3	SCN 2	SCN 1	SCN 0

SCN

Sets the scanning starting position of the gate driver.

Table 50. Gate Scan Position Control.

SCN[4:0]	Start Position	
	GS = 0	GS = 1
00000	G1	G160
00001	G9	G152
00010	G17	G144
---	---	---
10001	G137	G24
10010	G145	G16
10011	G153	G8

[Note]

Ensure that gate start position (SCN) + the number of LCD driver lines (NL) ≤ 160 when GS = 0, and that gate start position (SCN) - the number of LCD driver lines (NL) ≥ 0 when GS = 1

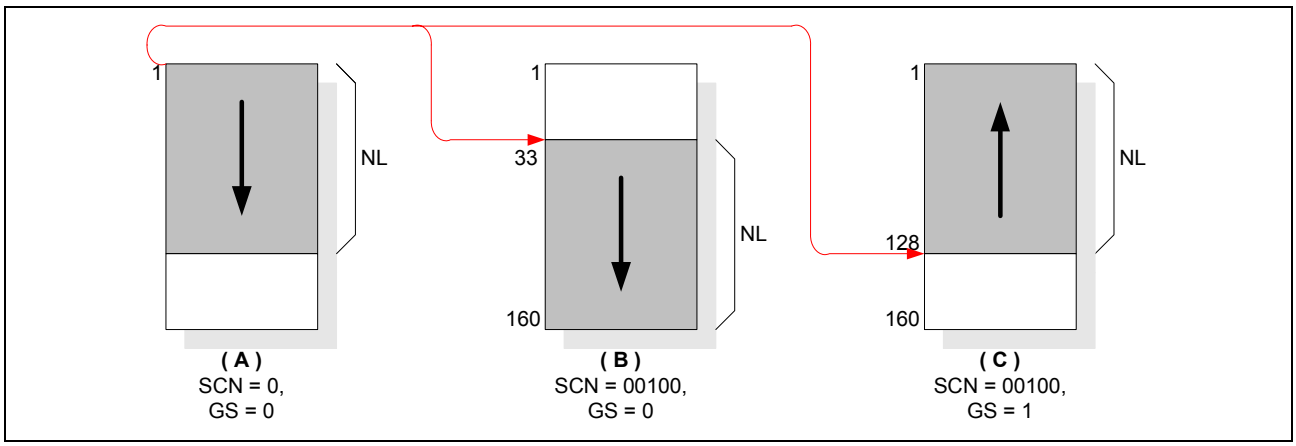


Figure 27. Gate scan position control

8.3.22. 1st & 2nd Screen driving position (R42h/R43h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	SE17	SE16	SE15	SE14	SE13	SE12	SE11	SE10	SS17	SS16	SS15	SS14	SS13	SS12	SS11	SS10
W	1	SE27	SE26	SE25	SE24	SE23	SE22	SE21	SE20	SS27	SS26	SS25	SS24	SS23	SS22	SS21	SS20

SS1

Specifies the starting position (or line) of the first display screen. The first screen displays starts from the SS1 + 1st line.

SE1

Specifies the end position (or line) of the first screen to be displayed. The screen display operation ends after the SE1 + 1st line has been written. For instance, when SS[7:0] = 07h and SE[7:0] = 10h, the screen displays payload images from G8 ~ G17 lines, The rest of the lines, from G1 ~ G7 and from G18 ~ the last line, displays either a black or white images depending on the value of PT register. Ensure that the following precondition is satisfied: SS1[7:0] ≤ SE1[7:0] ≤ 9Fh.
For details, refer to Split Screen Driving Function section, which will be described later.

SS2

Specifies the starting position (or line) of the second display screen. The second screen displays from SS2 + 1st line. It is displayed when SPT = 1.

SE2

Specifies the end position (or line) of the second screen to be displayed. The screen display operation ends after the SE2 + 1st line has been written. For instance, when SS2[7:0] = 20h, SE2[7:0] = 4Fh and SPT = 1, the screen displays payload images from G33 ~ G80 lines. Ensure that the following precondition is satisfied: 00h ≤ SS1[7:0] ≤ SE1[7:0] ≤ SS2[7:0] ≤ SE2[7:0] ≤ 9Fh.
For details, refer to Split Screen Driving Function section, which will be described later.

8.3.23. Horizontal & Vertical RAM address position (R44h/R45h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	HEA 7	HEA 6	HEA 5	HEA 4	HEA 3	HEA 2	HEA 1	HEA 0	HSA 7	HSA 6	HSA 5	HSA 4	HSA 3	HSA 2	HSA 1	HSA 0
W	1	VEA 7	VEA 6	VEA 5	VEA 4	VEA 3	VEA 2	VEA 1	VEA 0	VSA 7	VSA 6	VSA 5	VSA 4	VSA 3	VSA 2	VSA 1	VSA 0

VSA, VEA

Specifies the vertical start/end positions of a window for access to the specified partial memory (Window). Data can be written to GRAM from the address specified by VEA[7:0] to the address specified by VSA[7:0]. Note that the Window Addresses must be set before GRAM is updated. Ensure that the following precondition is satisfied: 00h ≤ VSA[7:0] ≤ VEA[7:0] ≤ 9Fh. See Figure 28.

HSA, HEA

Specifies the horizontal start/end positions of a Window for access to the specified partial memory (Window). Data can be written to GRAM from the address specified by HSA[7:0] to the address specified by HEA[7:0]. Note that the Window Addresses must be set before GRAM is updated. Ensure that the following precondition is satisfied: 00h ≤ HSA[7:0] ≤ HEA[7:0] ≤ 7Fh. See Figure 28.

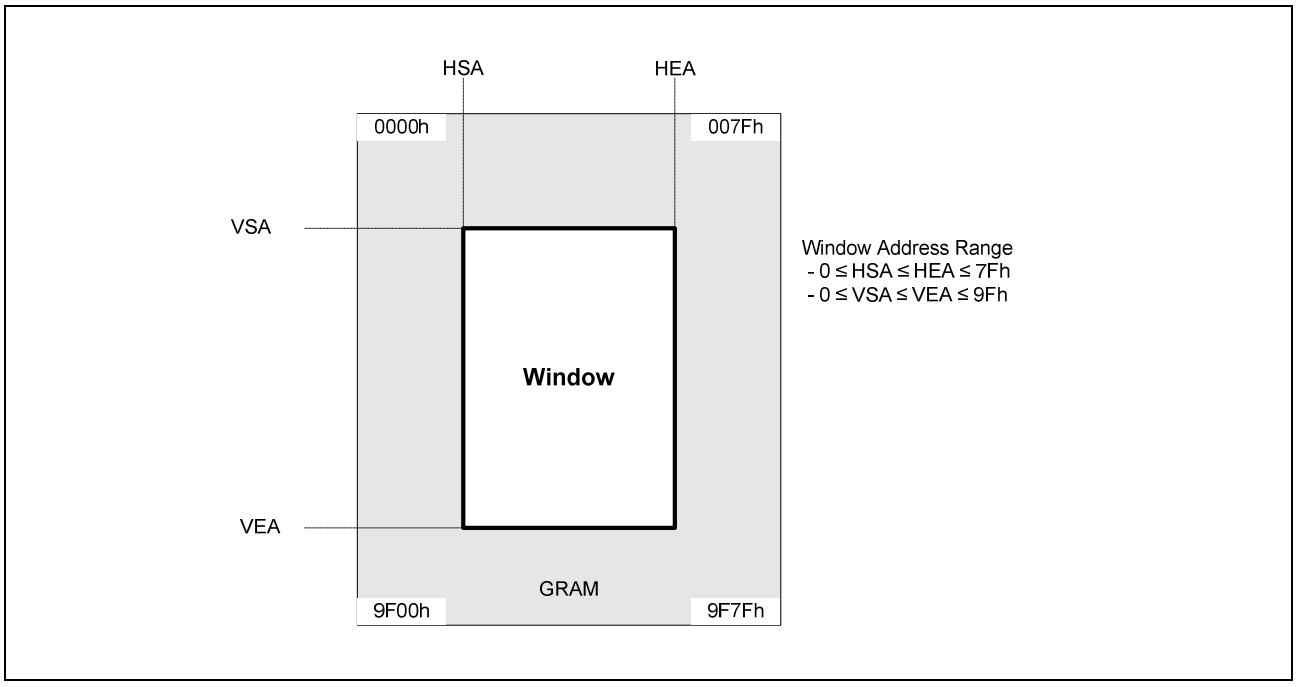


Figure 28. Window address function

[Note] Ensure that the Window addresses are within the GRAM address space.

■ Split screen driving function

The S6D0151 can select and drive two screens at any position with the screen-driving position registers. The two screens can be selectively driven to reduce power consumption.

For the 1st divided screen, start line and end line are specified by the 1st screen-driving position registers (SS1[7:0], SE1[7:0]). For the 2nd division screen, start line and end line are specified by the 2nd screen-driving position registers (SS2[7:0], SE2[7:0]).

The 2nd screen control is enabled when SPT is set to 1. The total count of selection-driving lines for the 1st and 2nd screens must correspond to the LCD-driving duty set value.

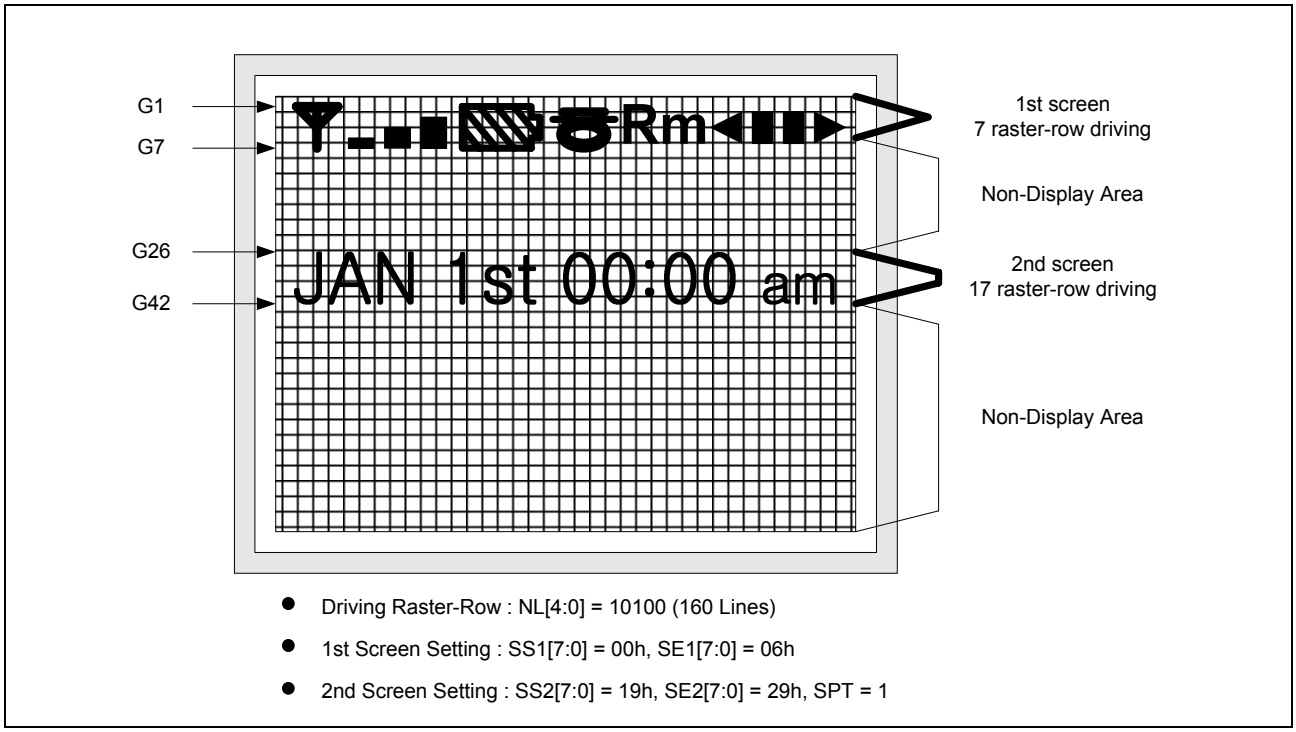


Figure 29. Split screen driving function

■ **Examples of split screen driving function**

Table 51. Split Screen Driving Function with SPT = 0.

Register Value	Display Operation
SE1[7:0] – SS1[7:0] = NL	Full screen display Normally displays from SS1[7:0] to SE1[7:0]
SE1[7:0] – SS1[7:0] < NL	Partial display Normally displays from SS1[7:0] to SE1[7:0] Black or White image is displayed according to the PT setting in the remaining area (GRAM data is not related at all)
SE1[7:0] – SS1[7:0] > NL	Not available

[Note] SS2[7:0] and SE2[7:0] are ignored

Table 52. Split Screen Driving Function with SPT = 1.

Register Value	Display Operation
SE1[7:0] – SS1[7:0] + SE2[7:0] – SS2[7:0] = NL	Full screen display Normally display from SS1[7:0] to SE2[7:0]
SE1[7:0] – SS1[7:0] + SE2[7:0] – SS2[7:0] < NL	Partial display Normally displays from SS1[7:0] to SE1[7:0] and from SS2[7:0] to SE2[7:0] Black or White image is displayed according to the PT setting in the remaining area (RAM data is not related at all)
SE1[7:0] – SS1[7:0] + SE2[7:0] – SS2[7:0] > NL	Not available

■ Partial display setup flow

A flow diagram describing the set up procedure for Partial Display operation is shown in Figure 30. It is possible to determine the output levels of the driver in Non-Display Area (the area outside of partial display), so one can select appropriate level depending on the panel's condition.

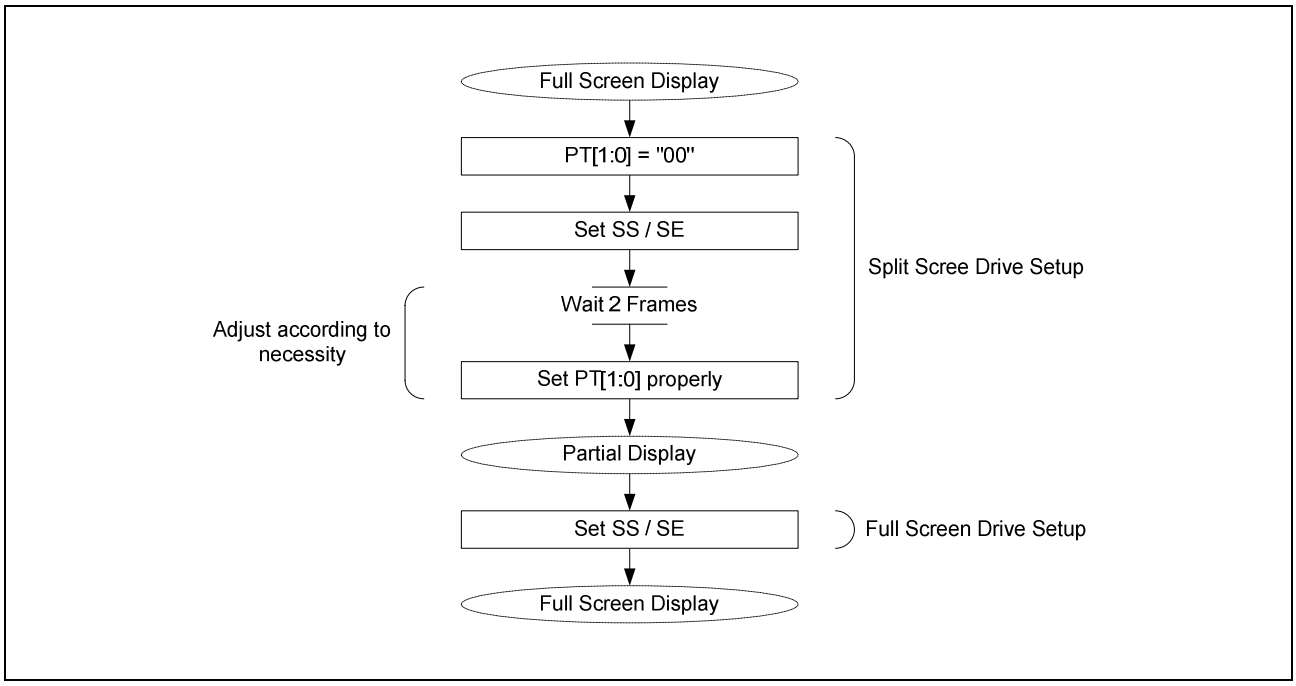


Figure 30. Partial display set-up flow

■ Data update with window address function

When data is written to the internal GRAM, the window that is specified by the horizontal address registers (HSA[7:0], HEA[7:0]) and the vertical address registers (VSA[7:0], VEA[7:0]) can be updated consecutively. Data is written in the direction specified by AM (horizontally / vertically) and ID (incrementally / decrementally). Thus when image data, is being written, data can be written consecutively without explicitly being worried about causing a data warp.

The window must be specified to be within GRAM address area as described below and the start address for write must be set within the window.

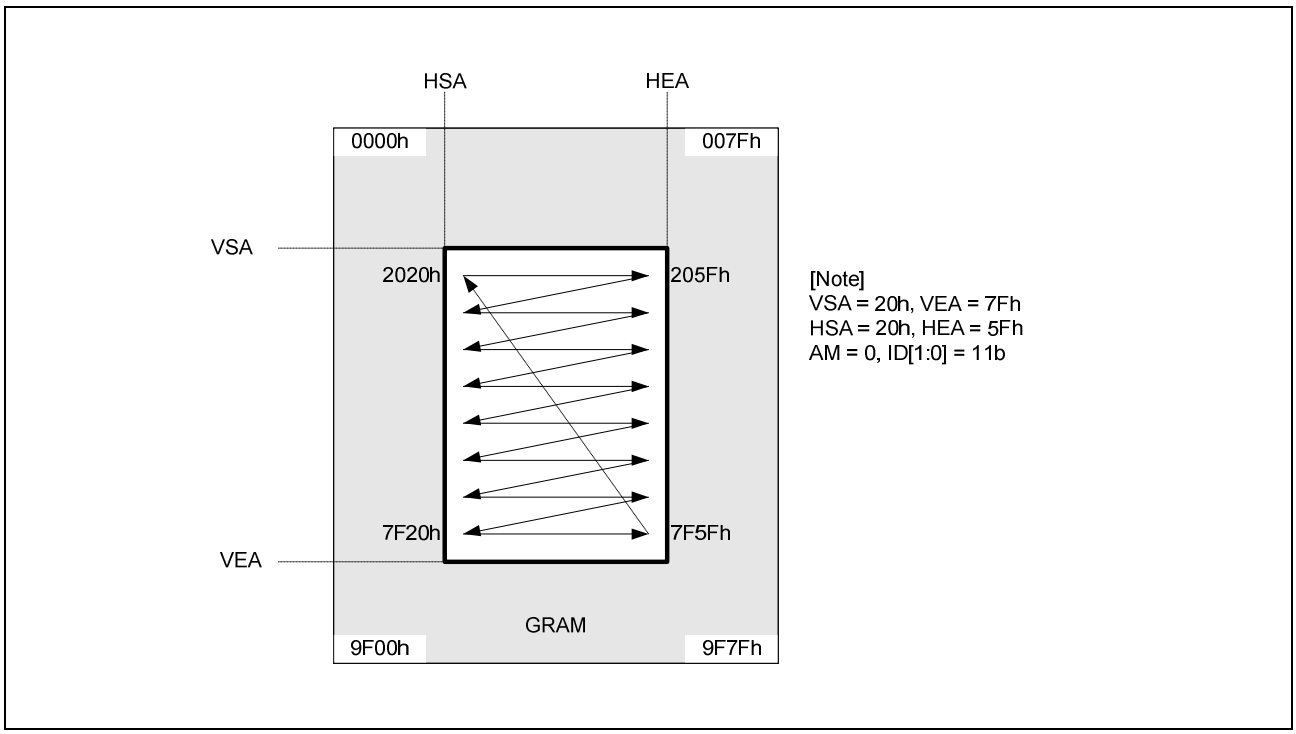


Figure 31. Example of data update with window address function

8.3.24. Oscillator control (R61h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	X	X	X	X	X	X	X	0	X	X	X	RADJ4	RADJ3	RADJ2	RADJ1	RADJ0

RADJ

Selects the frequency of internal oscillator.

Table 53. RADJ and Internal oscillator oscillation frequency.

RADJ[4:0]	Oscillation Speed	
00000	Not available	
:	Not available	
10000	Not available	
10001	x 0.768	Min.
10010	X 0.795	-
10011	x 0.823	-
10100	x 0.853	-
10101	x 0.885	-
10110	x 0.921	-
10111	x 0.958	-
11000	x 1.000	Default
11001	x 1.045	-
11010	x 1.095	-
11011	x 1.148	-
11100	x 1.210	-
11101	x 1.276	Max.
11110	Not available	
11111	Not available	

[Note] Setting example)If default oscillation frequency is 240kHz and the register setting of RADJ[4:0] is 10001, the internal oscillator oscillation frequency is 240kHz x 0.768 =184kHz.

8.3.25. DC/DC convert low power mode (R69h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	0	0	0	0	0	0	0	NLDC3	NLDC2	NLDC1	NLDC0	NLPM

NLPM

Sets DC/DC converter to Low power mode.

Table 54. VGH,VGL DC/DC converter operation mode.

NLPM	Operation mode
0	Normal operation mode
1	Low power mode

NLDC

Sets the operational clock speed of each DC/DC converter circuit for low power mode. (See Table 55)
Make sure that a precondition of NLPM=1 is satisfied.

Table 55. DC/DC converter1/3 operation for low power mode.

NLDC[1:0]	DC/DC converter1/3 operation clock
00	DCCLK/1
01	DCCLK/2
10	DCCLK/4
11	DCCLK/8

Table 56. DC/DC converter2 operation for low power mode

NLDC[3:2]	DC/DC converter2 operation clock
00	DCCLK/2
01	DCCLK/4
10	DCCLK/8
11	DCCLK/16

8.3.26. Source Driver pre-driving period setting (R70h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	X	X	X	X	X	X	X	X	SDT 1	SDT 0	X	X	X	X	EQ1	EQ0

This register determine the drive timings of the S6D0151.

EQ

EQ period is sustained for the number of clock cycles that is set in EQ1-0. When VcomL<0V, use AVDD-VcomL<6V or set these bits as 00 for preventing abnormal function.

Table 57. Equalization Control.

EQ	EQ Period Internal Operation (synchronized with internal clock)
00	No EQ
01	1 DISP_CK
10	2 DISP_CKs
11	3 DISP_CKs

[Note]

DISP_CK : OSCK_CK divided by DIV[1:0](DM = 2'b00) or DOTCLK divided by 8(DM = 2'b01 and RIM[1] = 1'b1)

f(EQ) + f(SDT) + f(GNO) < 15 DISP_CKs

SDT

Sets the amount of time delay from 1H start time to source output response time.

Table 58. Source Output Delay Control

SDT	Delay Amount of the Source Output
00	1 DISP_CK
01	2 DISP_CKs
10	3 DISP_CKs
11	4 DISP_CK s

[Note]

DISP_CK : OSCK_CK divided by DIV[1:0](DM = 2'b00) or DOTCLK divided by 8(DM = 2'b01 and RIM[1] = 1'b1)

f(EQ) + f(SDT) + f(GNO) < 15 DISP_CKs

For detail, refer to Panel Control Interface mode, which will be described later.

8.3.27. Gate Output Period Control (R71h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	X	X	X	X	GNO1	GNO0	X	X	X	X	X	X	X	X	X	X

GNO

Controls the amount of non-overlap period between gate outputs.

Table 59. Non-Overlap Period Control.

GNO	Non-Overlap Period
00	2 DISP_CKs
01	4 DISP_CKs
10	6 DISP_CKs
11	8 DISP_CK s

[Note]

DISP_CK : OSCK_CK divided by DIV[1:0](DM = 2'b00) or DOTCLK divided by 8(DM = 2'b01 and RIM[1] = 1'b1)

f(EQ) + f(SDT) + f(GNO) < 15 DISP_CKs

8.3.28. Software Reset Control (R72h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	SR

SR

A user can reset the internal status of the S6D0151 by setting this register to 0. This register is automatically set to 1 after about 100ns.

8.3.29. Test_Key (R73h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	X	X	X	X	X	X	X	X	TEST_KEY[7:0]							

TEST_KEY

This register should be set to A5 if an update to MTP data is desired. After an MTP update, the value of this register should be changed to protect the MTP data from an accidental corruption.

8.3.30. DC/DC converter Clock Source Selection (RB3h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	`	0	0	0	X	0	1	0	X	X	X	DCR_EX	X	X	X	1

DCR_EX

Selects the source of DC/DC converter clock. In RGB mode, DCR_EX should be set before the power setting.

Table 60. DC/DC Converter Clock Control.

DCR_EX	Source of the DC/DC converter clock
0	Internal Oscillator Clock
1	External DOTCLK

8.3.31. MTP Control (RB4h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	X	X	X	MTP_SEL	X	X	X	MTP_INIT	X	X	X	MTP_WRB	X	X	X	MTP_LOAD

MTP_LOAD

A user can load MTP data into internal register by writing 1 to this register before reading.

MTP_WRB

A user can write MTP data by writing 0 to this register.

MTP_INIT

A user can initialize MTP data by writing 1 to this register.

MTP_SEL

A user can use MTP data to control VCOMH.

Table 61. VCOMH Control.

MTP_SEL	VCOMH Control Data
0	VCM Register
1	MTP data

8.3.32. Module Vendor (RB6h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
R/W	1	TEST_IN4	TEST_IN3	SD_EN (0)	SD3 (0)	SD2 (0)	SD1 (0)	PSMD1 (0)	PSMD0 (1)	X	X	**1**	**1**	**1**	**1**	**1**	**1**

TEST_IN4, TEST_IN3

The identity of the module vendor can be found out by accessing this register. The value of this register depends on the external connections to TEST_IN[4:3] pads.

Table 62. Module Vendor.

Pad Connection		Read-out value of RB6h
TEST_IN[4]	**TEST_IN[3]**	
Tie to VSS	Tie to VSS	013fh
Tie to VSS	Tie to VDD3	413fh
Tie to VDD3	Tie to VSS	813fh
Tie to VDD3	Tie to VDD3	c13fh
Floating	Floating	013fh

SD_EN

Sets DC/DC converter to Schottky diode free mode.
Set this register to “1” before AP2-0 setting. For further information about timing, refer to Timing Digram of Power Setting section.

SD1

Selects input levels of DC/DC converter 2. Make sure that a precondition of SD_EN=1 is satisfied.
Set this register to “1” before AP2-0 setting in Schottky diode free mode. SD1 controls input levels of DC/DC converter2 with specific timing sequence. For further information about timing, refer to Timing Digram of Power Setting section.

Table 63. Input level of DC/DC converter2

SD1	Input Level of DC/DC Converter2 (VGH/L)	
	VCI1 Port	**AVDD Port**
0	VCI1	AVDD
1	GND → VCI1	GND → AVDD

SD2

Controls resistance of DC/DC converter2 input path. Make sure that a precondition of SD_EN=1 is satisfied. Set this register to “1” after PON setting in Schottky diode free mode. For further information about timing, refer to Timing Digram of Power Setting section.

Table 64. Start-up resistance control of DC/DC converter2

SD2	Resistance of DC/DC Converter2 (VGH/L) input path
0	> 100 ohm
1	< 50 ohm

SD3

Selects discharge path of parasitic BJT turn-on current during the start-up operation of DC/DC converter2. Make sure that a precondition of SD_EN=1 is satisfied.

Set this register to “1” before AP setting in Schottky diode free mode. For further information about timing, refer to Timing Digram of Power Setting section.

Table 65. Start-up discharge path control of DC/DC converter2

SD3	Path for discharge
0	External Schottky diode
1	Internally discharge

PSMD

Selects power-on delay time of the DC/DC converters.

Table 66. Power-on delay control.

PSMD[1:0]	Td (Refer to Figure 32)
00	2840*(1/fosc)
01	5680*(1/fosc)
10	11360*(1/fosc)
11	11360*(1/fosc)

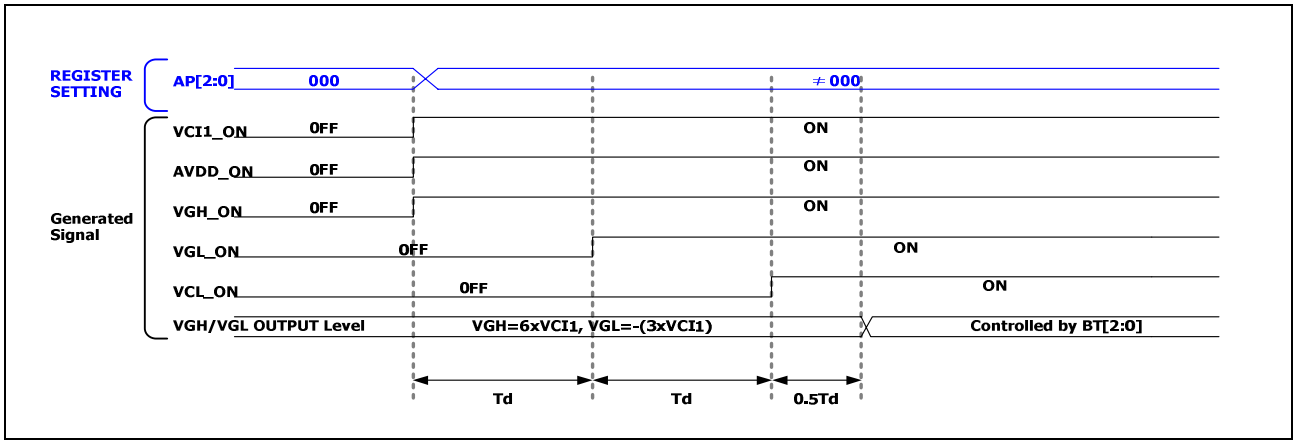


Figure 32. Power On Delay Control

8.3.33. MTP Data Read (RBDh)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
R/W	1	X	X	X	X	X	X	X	DISEN	X	MTP_DOUT[6:0]						

DISEN

Determines operational state of standby-mode discharge circuit.

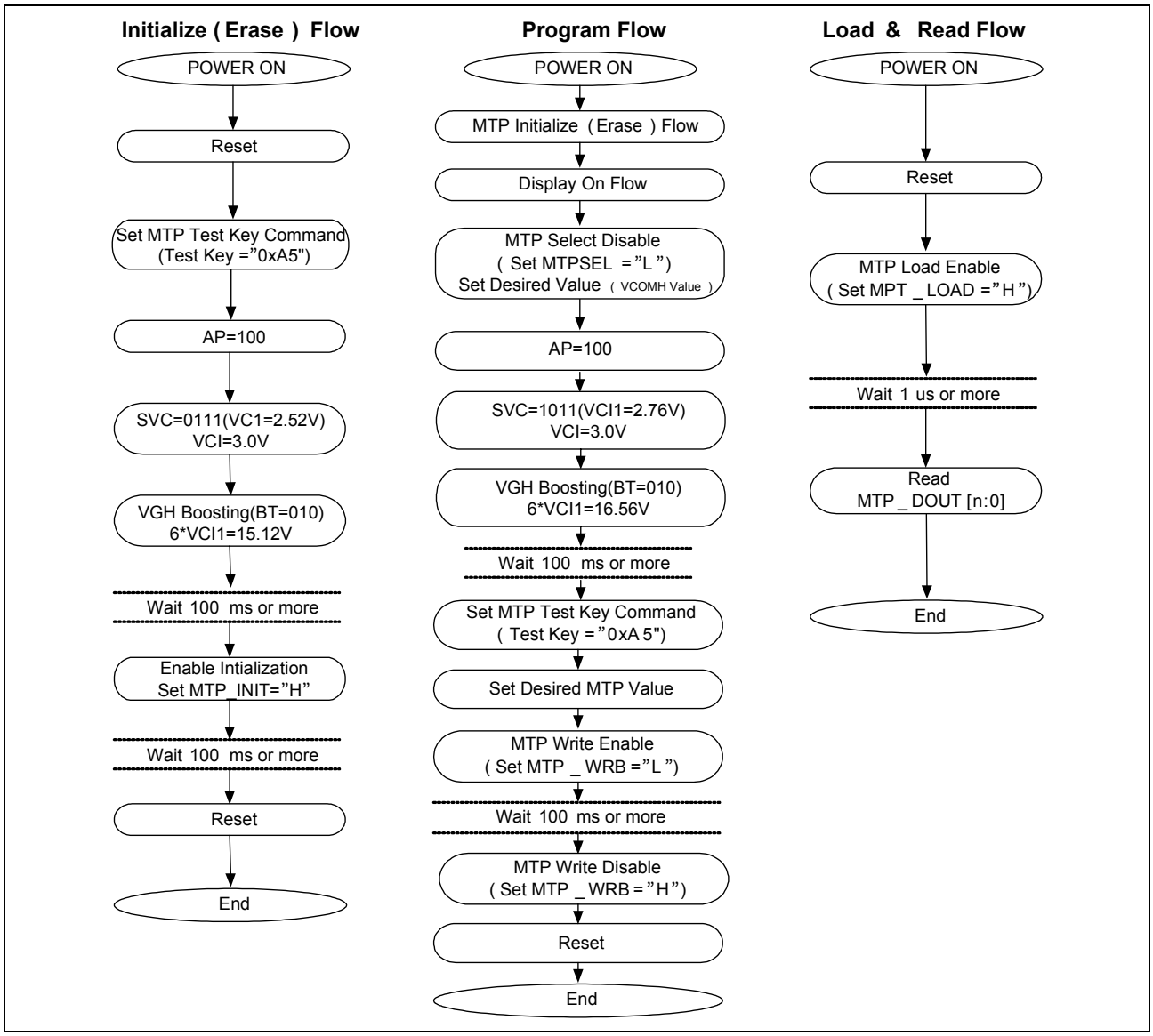
Table 67. Discharge Circuit Operation.

DISEN	VGL/VCL discharge circuit operation
0	Disable discharge circuit operation
1	Enable discharge circuit operation

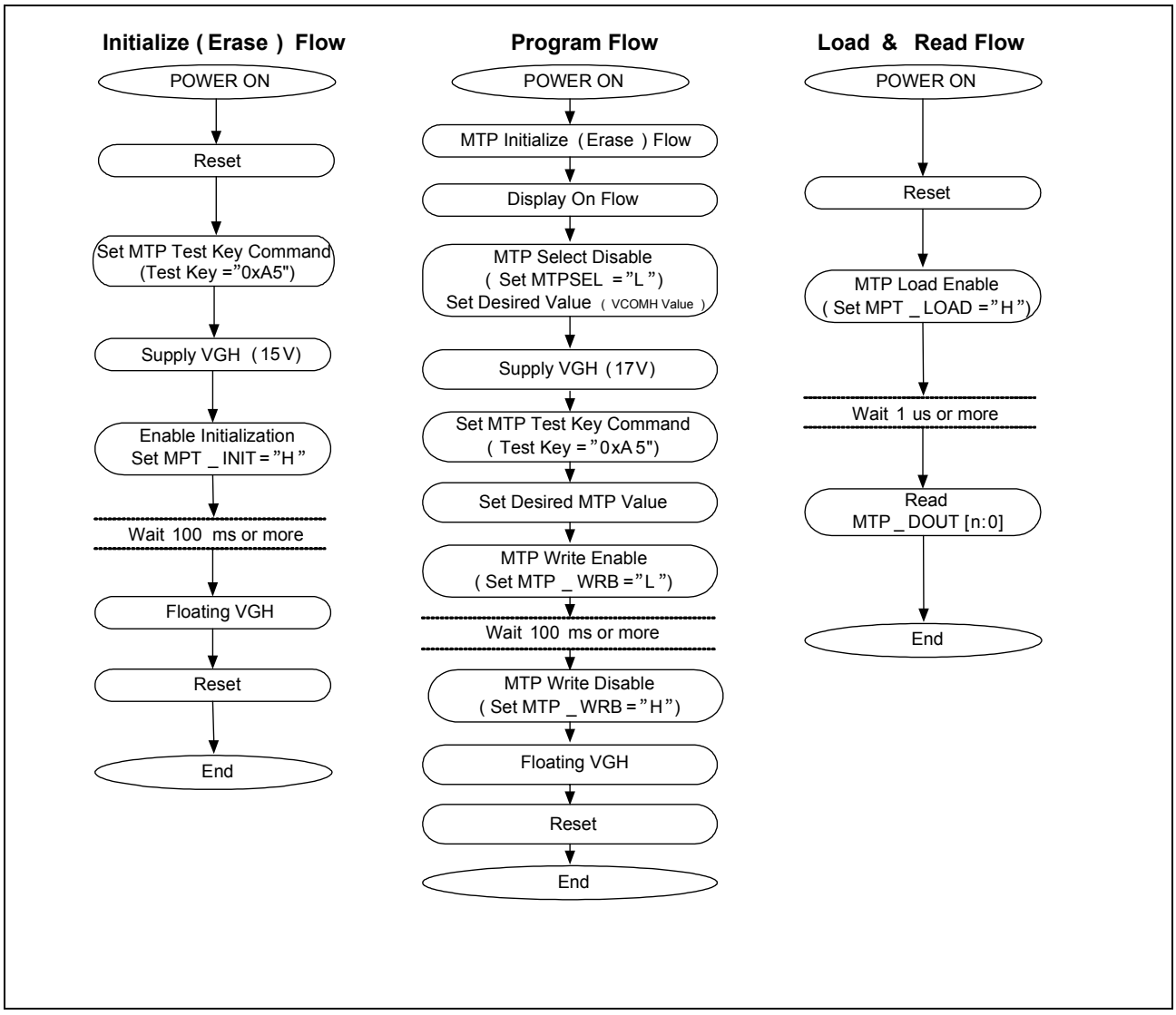
MTP_DOUT

Stores MTP data read in the last MTP read operation.

MTP Control in Internal Mode



MTP Control in External Mode



Timing of MTP Control

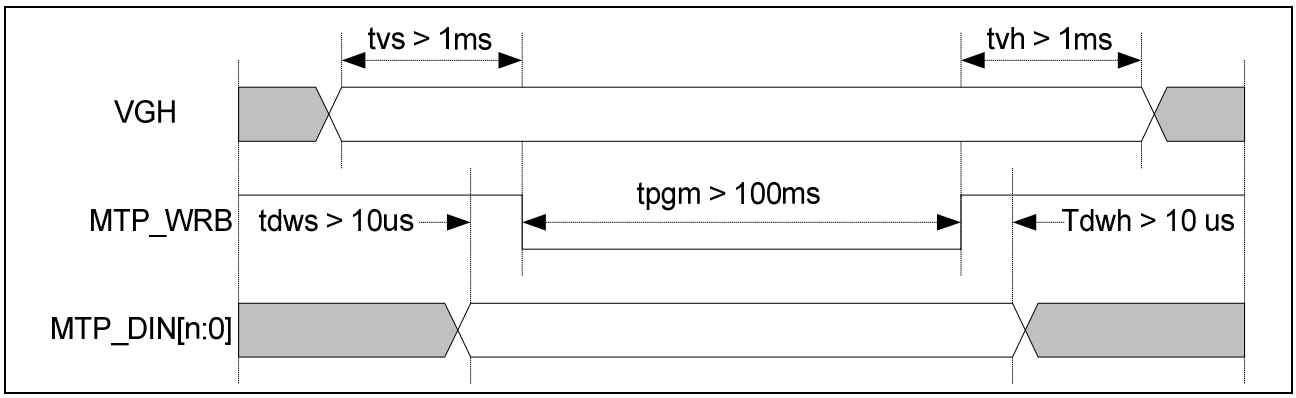


Figure 33. Voltage and waveforms for MTP programming.

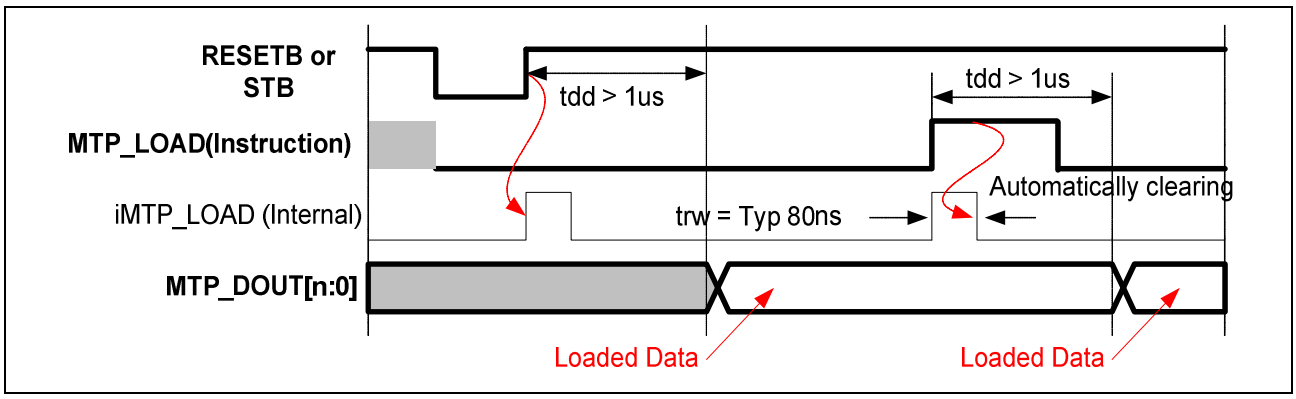


Figure 34. Timing of MTP Load.

Table 68. MTP writing time

(Refer to Figure 33.)

Timing	Min	Max	Unit
tvs	1	-	ms
tvh	1	-	ms
tdws	10	-	us
tdwh	10	-	us
tpgm	100	200	ms

Table 69. VGH(MTP Power) Voltage Tolerance.

Item	Pgm	Min	Typ	Max	Unit
Tolerance of VGH	Initial/Erase	14.5	15.0	15.5	V
	Write	16.5	17.0	17.5	V

Table 70. Current consumption during the period in which MTP is set.

Item	Symbol	Condition	Min	Typ	Max	Unit
Current consumption while MTP is set	I_{MTP}	VGH(init) = 15.5V	-	-	0.6	mA
		VGH(pgm)=17.5V	-	-		

[Note] This value is based on simulation for VDD3=2.8V, & VCI=2.8V

8.3.34. Interface Mode Selection (RBEh)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	X	X	X	X	X	X	X	X	X	X	X	IM_SEL	IM_3	X	X	FLM_MSK

IM_SEL

IM_SEL bit selects interface mode. If IM_SEL=0 then the mode of interface is selected by the settings on IM[3:0] pads, but if IM_SEL=1 then the mode is selected by the settings on IM_3 bit and IM[2:0] pads. In SPI mode, the use of IM_SEL is prohibited. The initial value of IM_SEL is 0.

Table 71. Interface mode selection.

IM_SEL	Interface mode is selected by
0	IM[3:0] pads
1	IM_3 bit, IM[2:0] pads

IM_3

IM_3 bit can determine the interface mode only if IM_SEL is set to 1. The initial value of IM_3 is 0.

FLM_MSK

When FLM_MSK is 1, it fixes the output of TEST_OUT[0] pad (=FLM signal) to 0.
The initial value of FLM_MSK is 0.

9. DC/DC converter

9.1. DC/DC converter circuit

The following figure shows the configuration of voltage generation circuit for the S6D0151. The DC/DC converter block consists of 3 converters. The first converter (DC/DC converter1) doubles the input voltage, VCI1, which is then boosted by the factors of X2, X2.5, X3 in the second converter (DC/DC converter circuit2). The third converter (DC/DC converter3) reverses boosting direction by generating the negative voltages of VCI1 magnitude; the resulting voltage is named as VCL. These DC/DC converter blocks generate following power supplies: AVDD, VGH, VGL, and VCL.

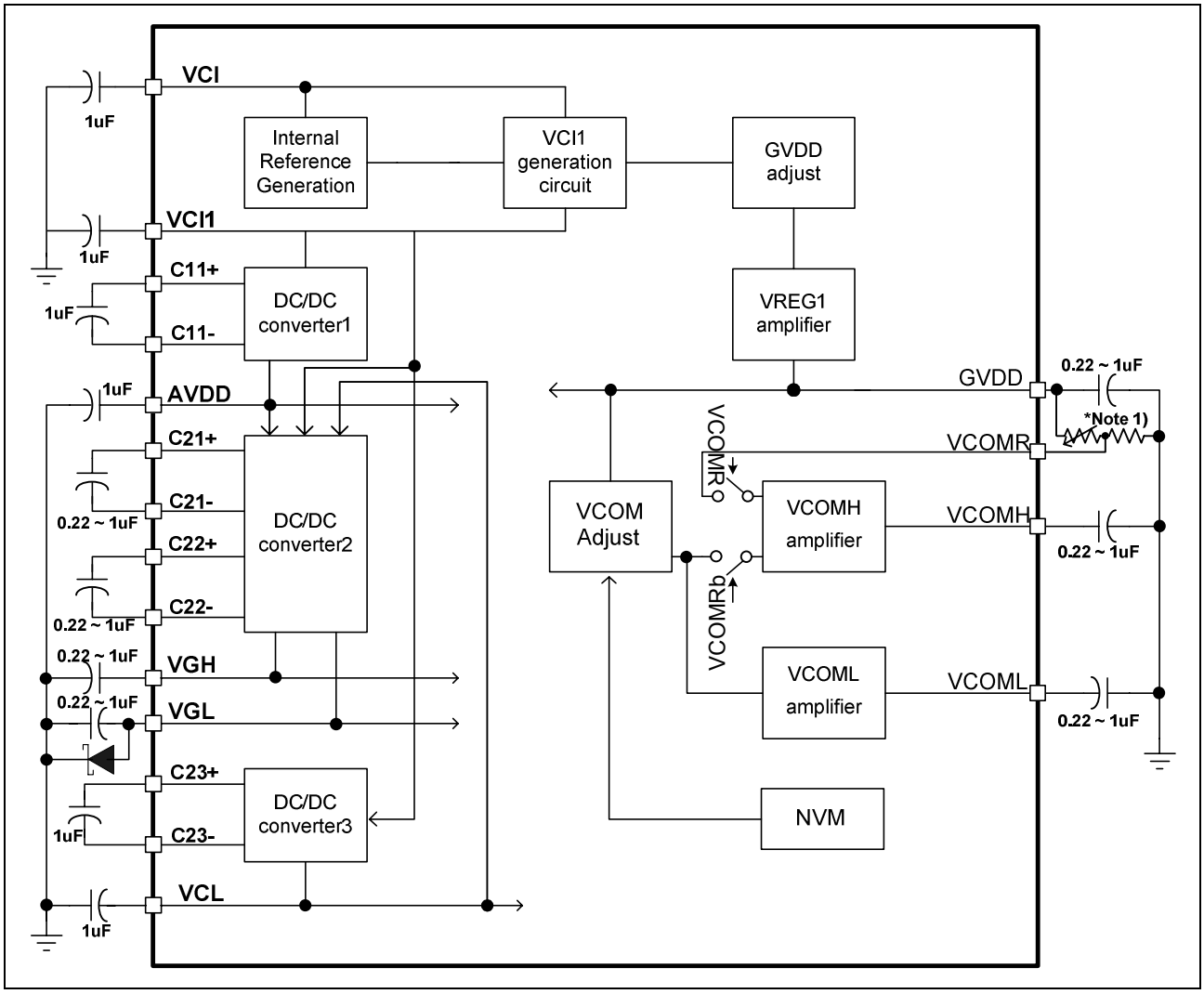


Figure 35. Configuration of the internal power-supply circuit.

[Note1]

When VCOMH is externally adjusted, attach these resistors. The total resistance should be higher than 100 kilo-ohm.

9.2. Pattern diagram for DC/DC converter voltage setting

The following figure shows a pattern diagram for the voltage setting and an example of waveforms.

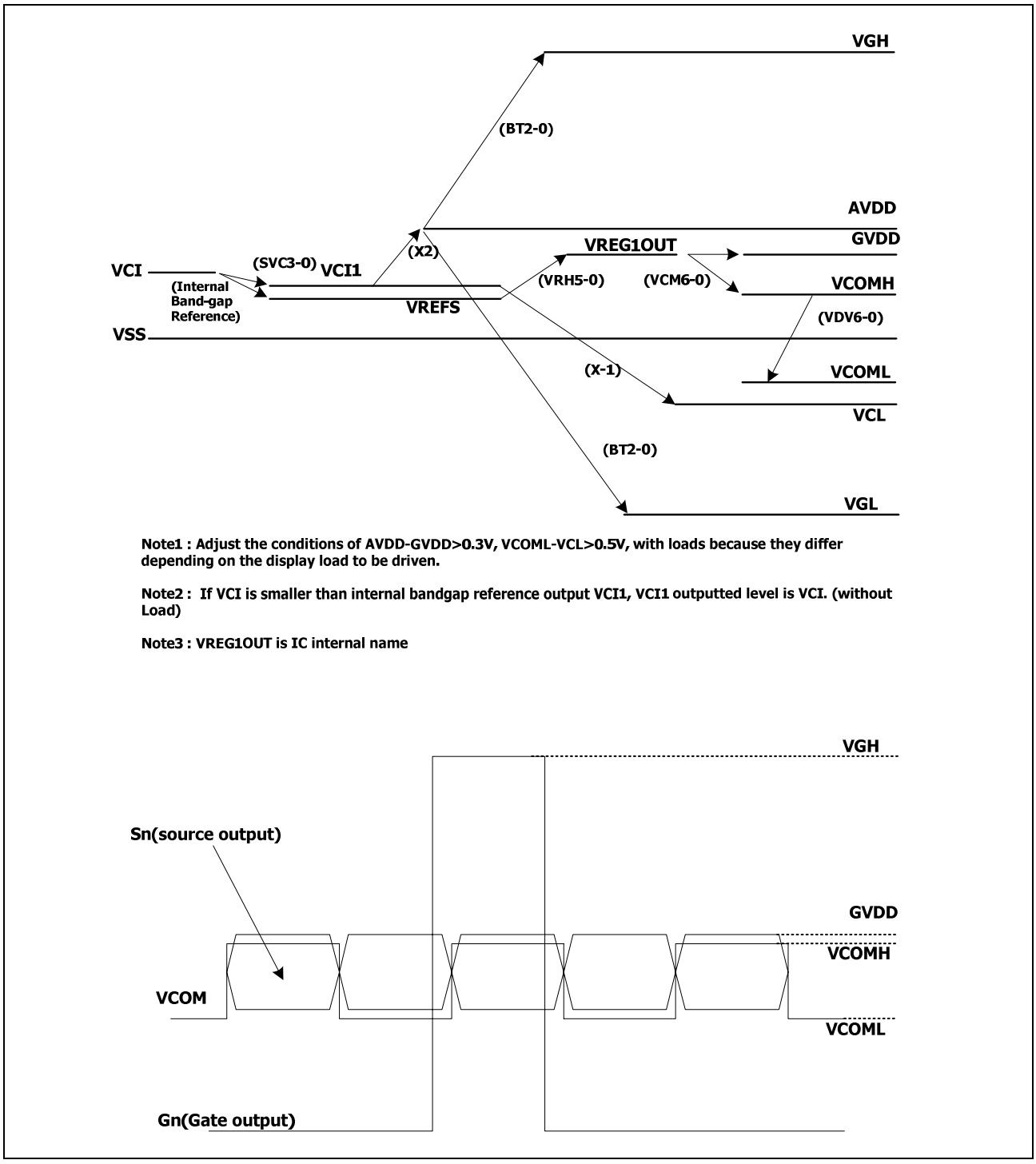


Figure 36. Pattern diagram and an example of waveforms.

9.3. Setup Flow of Power Supply

Apply the power in a sequence as shown in the following figure. The stable time of the oscillation circuit, step-up circuit, and operational amplifiers depend on the values of external resistors or capacitors.

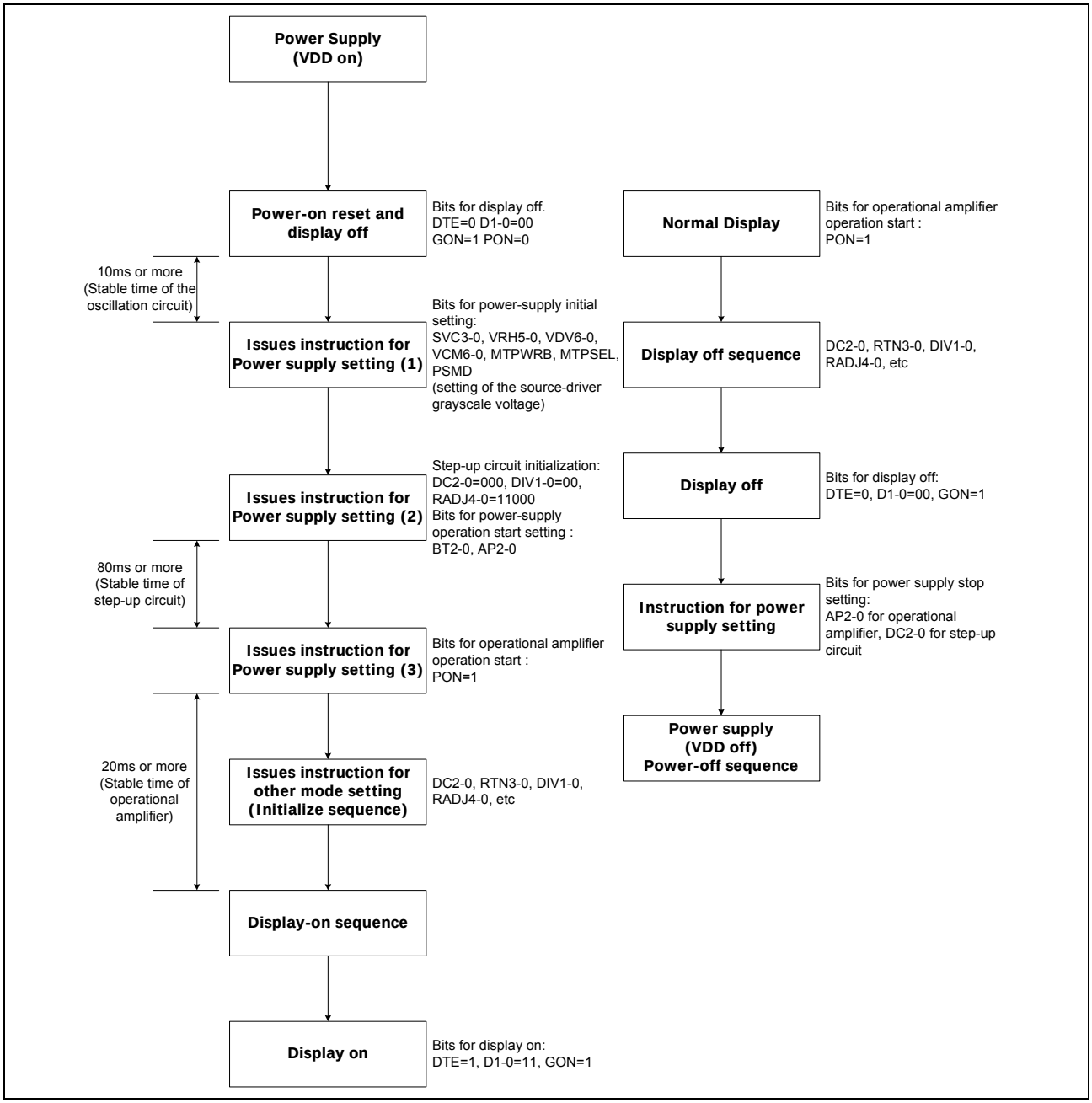


Figure 37. Set up flow of power supply.

9.4. Timing Diagram of Power Setting

DC/DC converter circuitry of S6D0151 can operate without Schottky diode. For using S6D0151 without Schottky diode, adds the register settings – RB6h (SD_EN, SD3, SD2 and SD1), R12h (SVC3-0), R10h (BT2-0) and R14h (VCOMG). For further information about timing of register setting, refer to Figure 39.

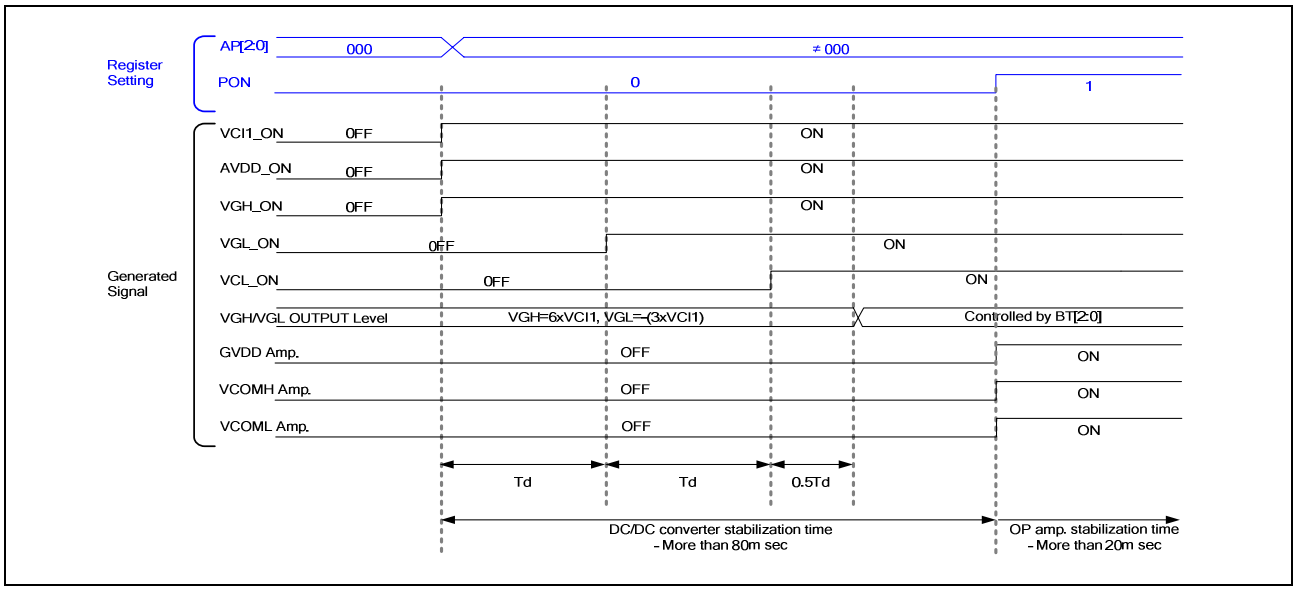


Figure 38. Set up flow of DC/DC conveter with Schottky diode.

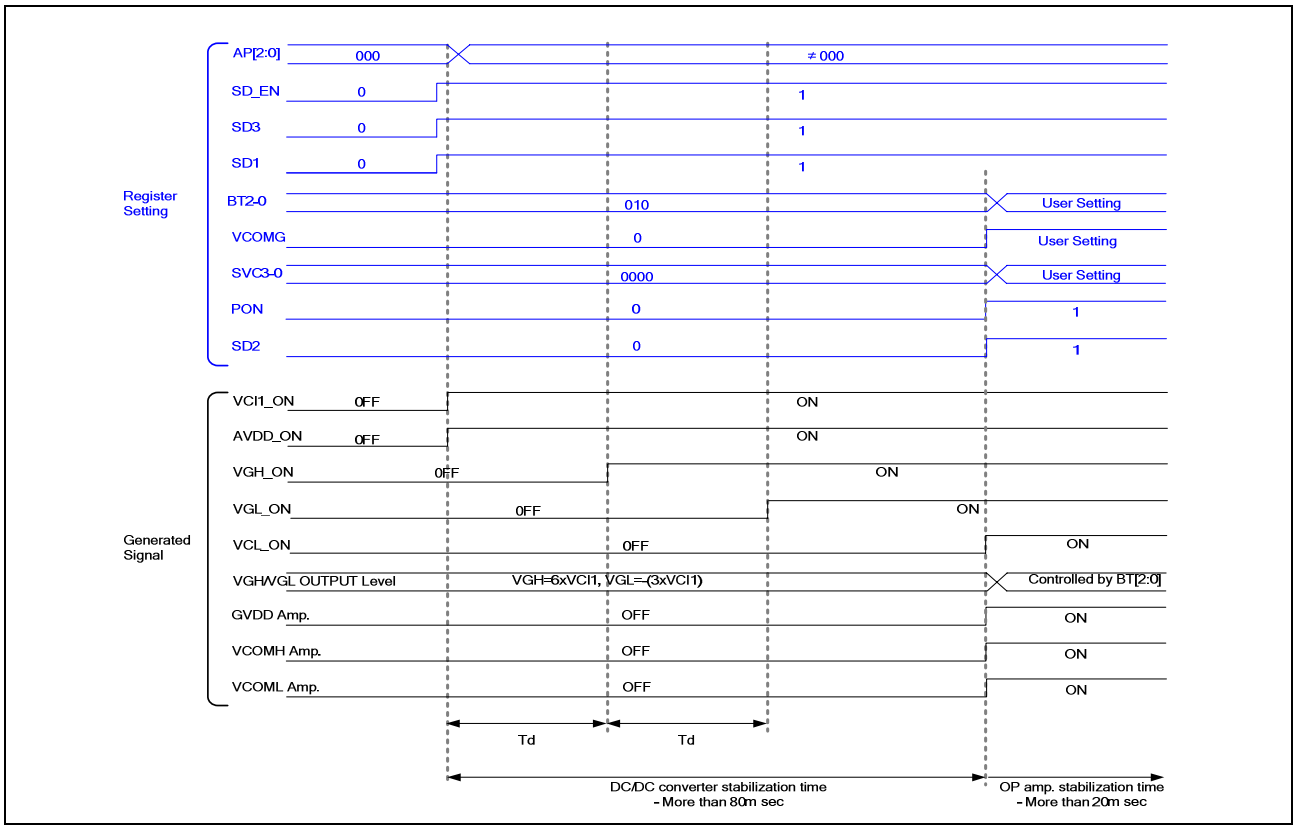


Figure 39. Set up flow of DC/DC conveter without Schottky diode.

9.5. Timing diagram of power-up/down sequence

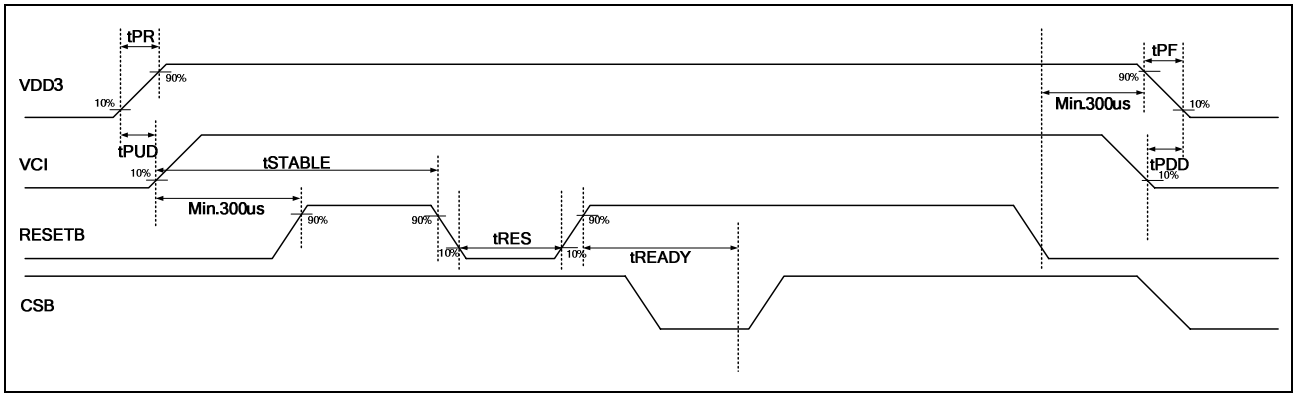


Table 72. AC characteristics for power-up/down sequence

Symbol	Parameter	Min.	Typ.	Max.	Unit
tPR	Power rise time	-	-	100	us
tPF	Power fall time	-	-	100	us
tSTABLE	Chip Stable	10	-	-	ms
tRES	Reset	20	-	-	us
tREADY	Chip initializing time after hardware reset	1	-	-	ms
tPUD	Power Up delay time	0	-	-	us
tPDD	Power Down delay time	0	-	-	us

9.6. Voltage regulation

The S6D0151 has one benefit of integrating voltage regulator that provides greater protection to internal logic circuits from damages originating from various noise events. An application setup for voltage regulation is shown in following figure.

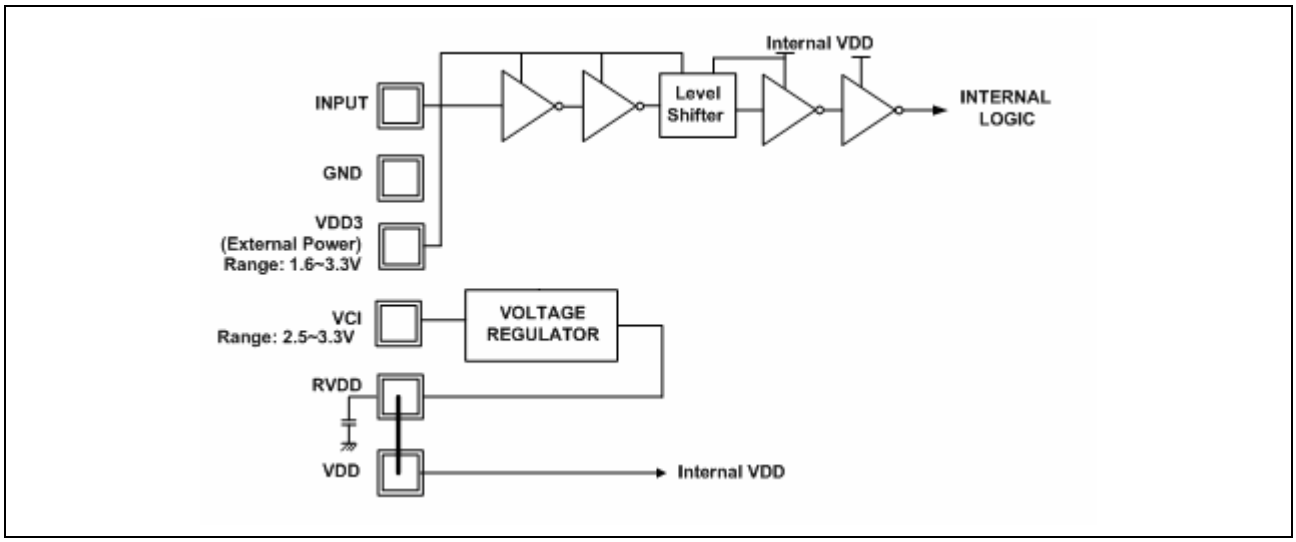


Figure 40. Voltage regulation function.

9.7. VCOM Setting

The S6D0151 provides three ways of adjusting VCOM amplitudes. The amplitude can be adjusted by means of an external resistor setting, an internal voltage divider, or MTP programmed setting.

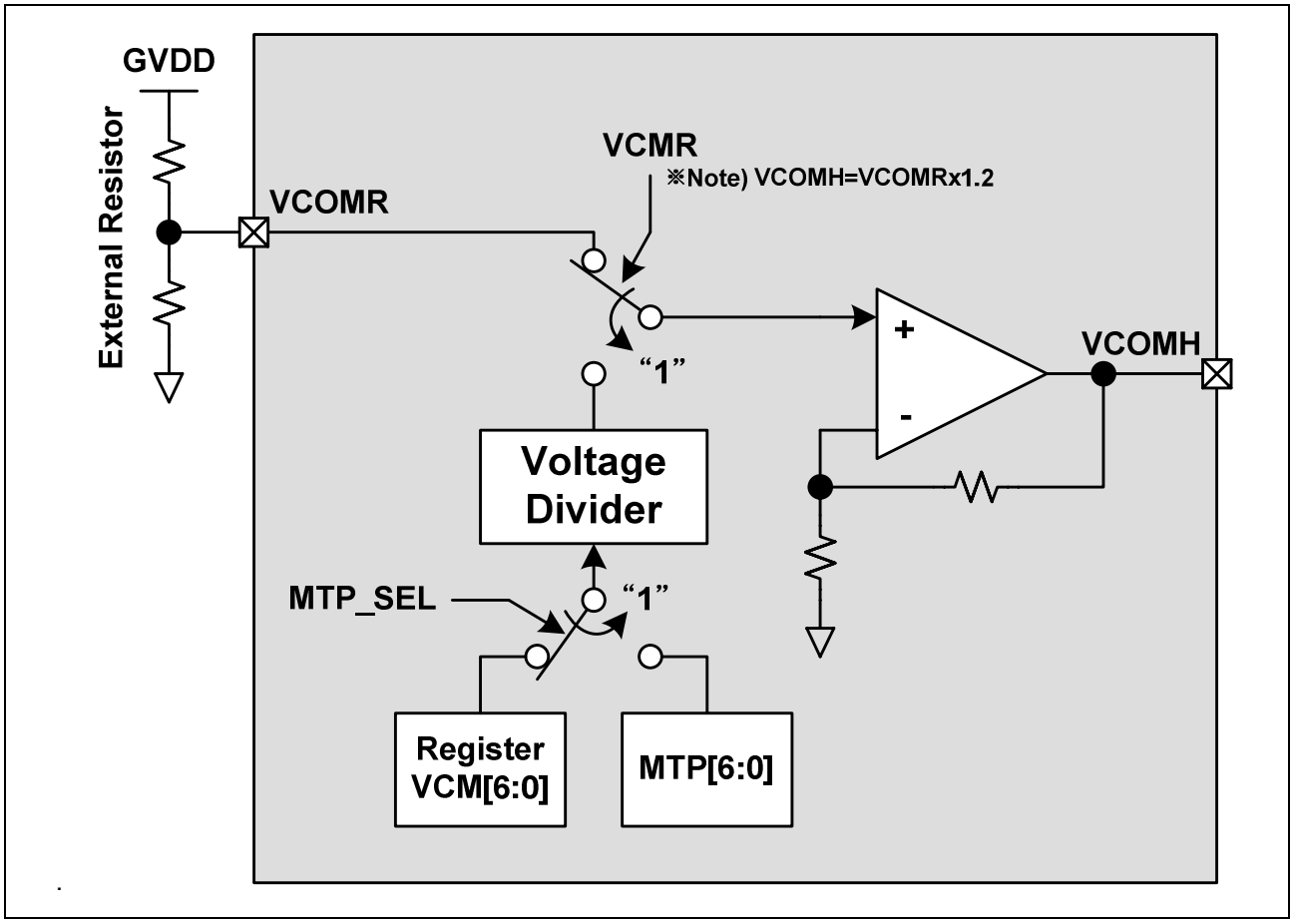


Figure 41. VCOMH control function.

10. Interface Specification

The S6D0151 incorporates nine types of CPU interface for transferring instructions and one type of RGB interface for displaying motion pictures. Selecting the proper interface for the screen data - motion or still picture – is critical for achieving efficient data transfers.

The External Clock Operation mode using RGB interface allows flicker-free screen updates. In this mode, the synchronization signals (VSYNC, HSYNC, and DOTCLK) are available for display operation. The display data (DB[17:0]) is transferred under the control of ENABLE in synchronization with VSYNC, HSYNC, and DOTCLK. Window Address function enables rewriting only to the internal GRAM area to display motion pictures. Using this function also enables simultaneously display of motion picture and previously written GRAM data.

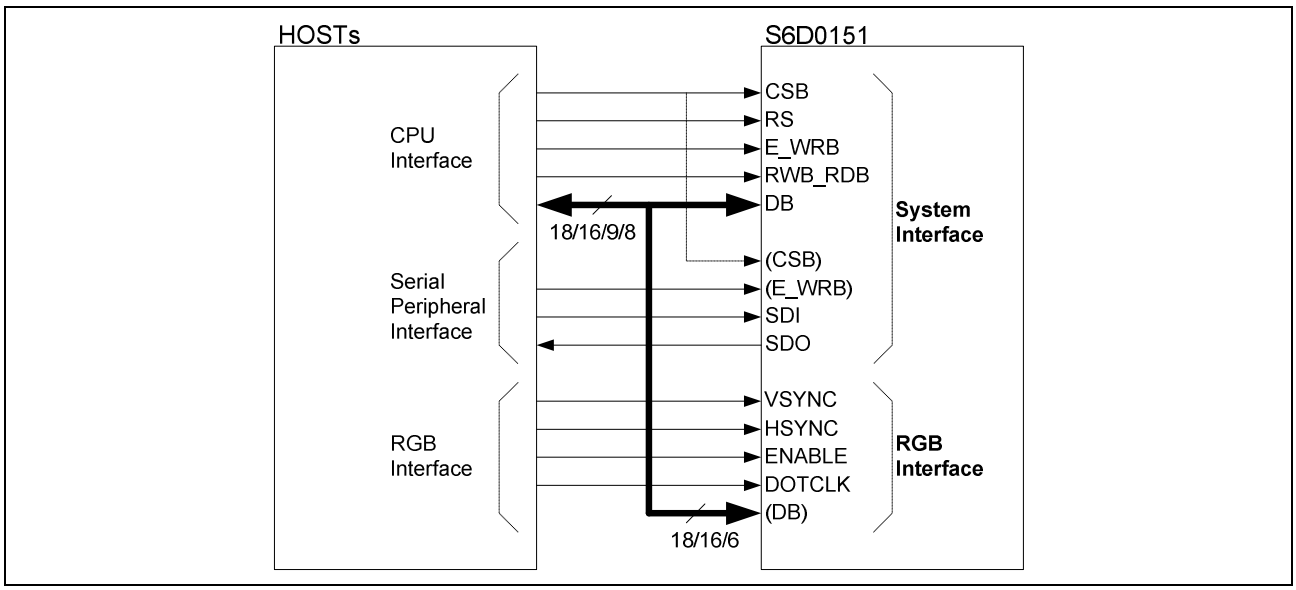


Figure 42. System interface and RGB interface.

10.1. System Interface

The S6D0151 has nine System Interfaces as shown below.

Table 73. System Interfaces of the S6D0151.

No	Description
1	68x-System 18-bit bus interface
2	68x-System 16-bit bus interface
3	68x-System 9-bit bus interface
4	68x-System 8-bit bus interface
5	80x-System 18-bit bus interface
6	80x-System 16-bit bus interface
7	80x-System 9-bit bus interface
8	80x-System 8-bit bus interface
9	4-/3-wire SPI (Serial Peripheral Interface)

Specific interface type is selected by IM[3:0]. For more detail, refer to Description of the Signal Pad section described earlier.

10.1.1. 68-Series 18-bit CPU interface

Bit Assignment

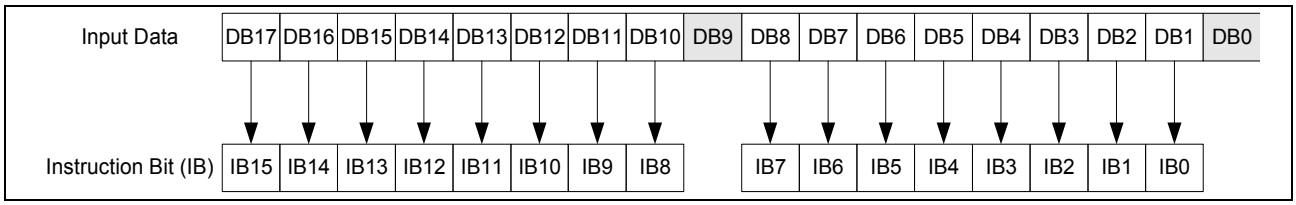


Figure 43. Bit assignment of instructions on 68-series 18-bit CPU interface.

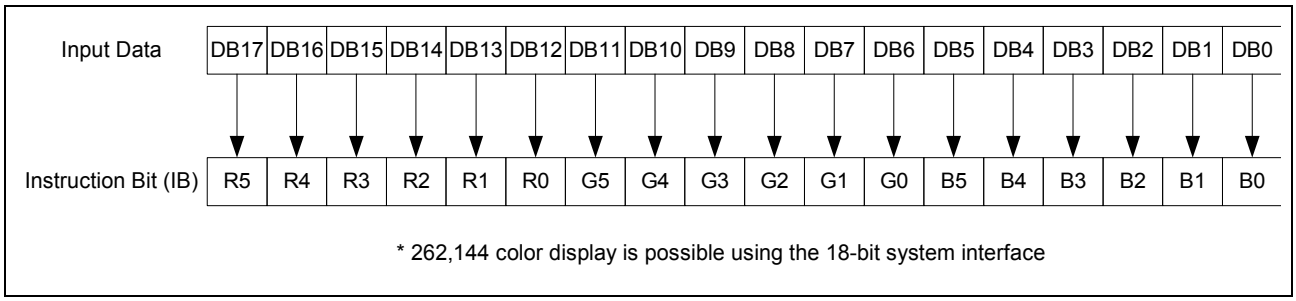


Figure 44. Bit assignment of GRAM Data on 68-Series 18-bit CPU Interface.

Timing Diagram

There are four timing conditions for 68 18-bit CPU interface: index write timing condition, data write timing condition, data read timing condition and status read timing condition.

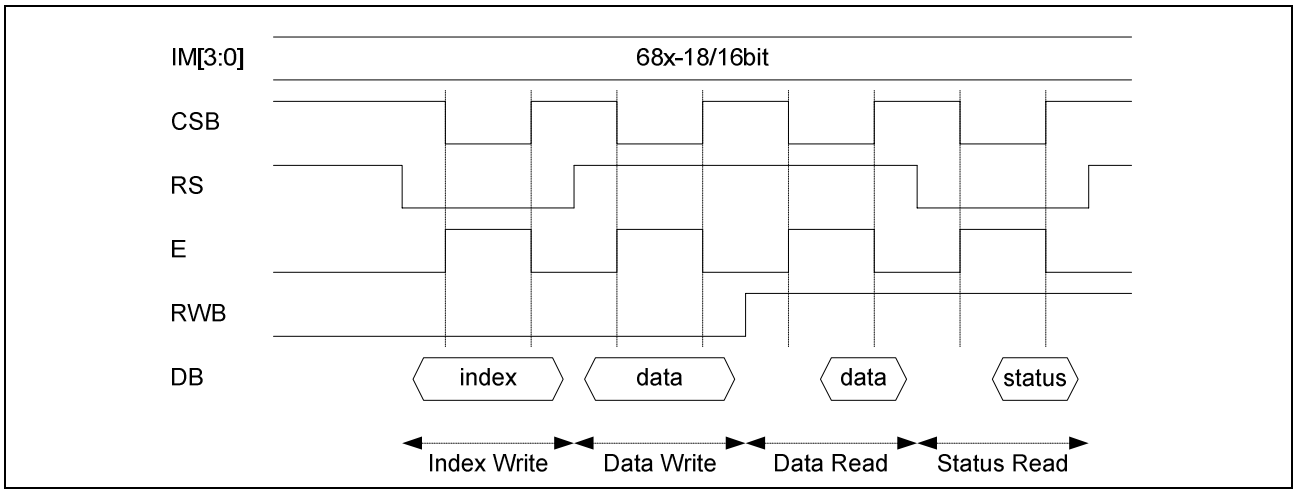


Figure 45. Timing Diagram of 68-Series 18-bit CPU Interface.

10.1.2. 68-Series 16-bit CPU interface

Bit Assignment

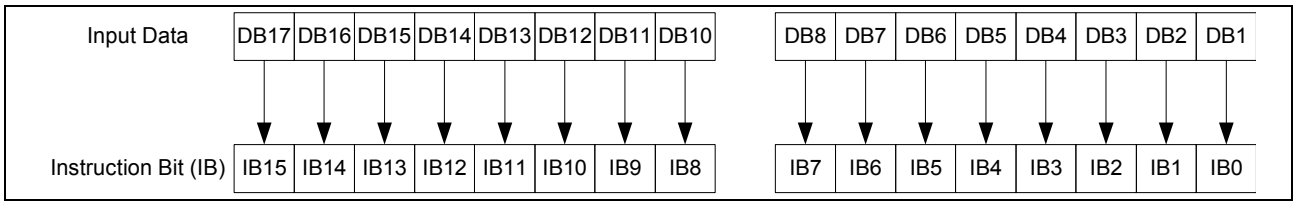


Figure 46. Bit Assignment of Instructions on 68-Series 16-bit CPU Interface.

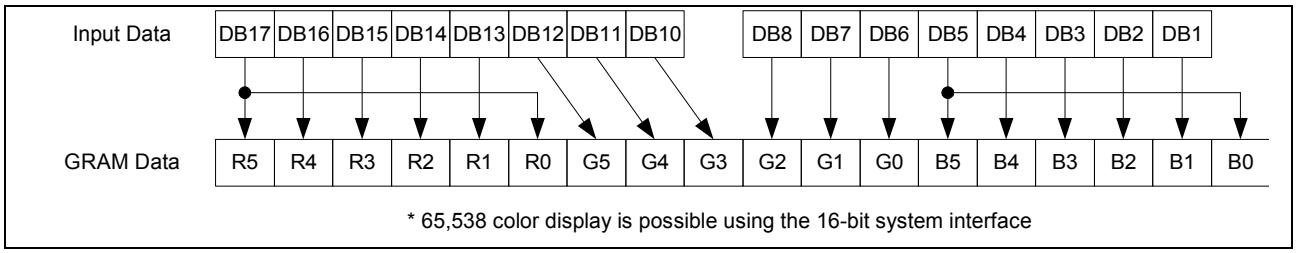


Figure 47. Bit Assignment of GRAM Data on 68-Series 16-bit CPU Interface.

Timing Diagram

There are four timing conditions for 68-Series 16-bit CPU interface: index write timing condition, data write timing condition and status read timing condition.

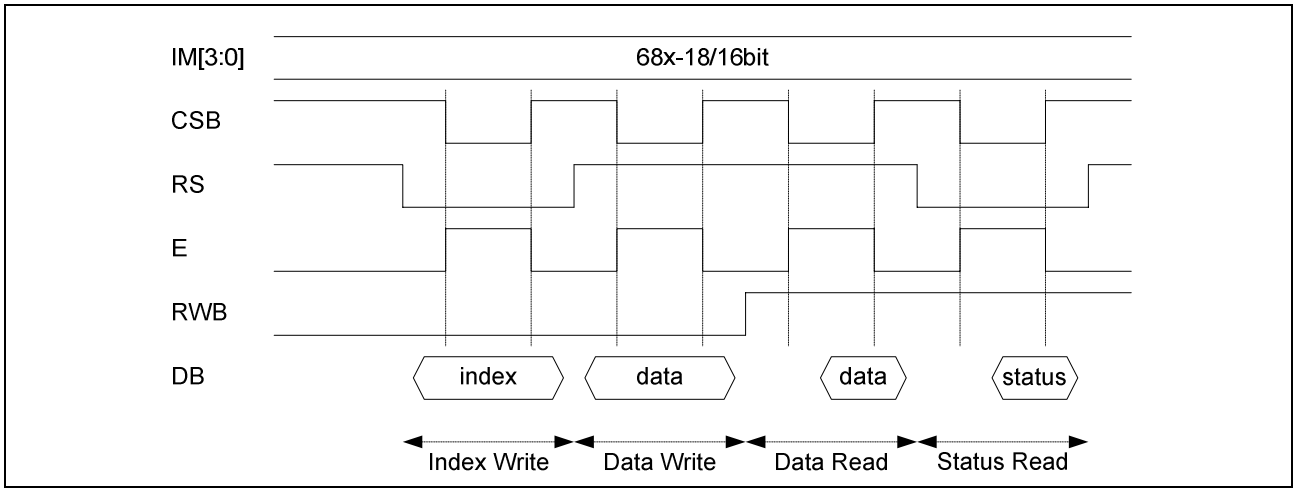


Figure 48. Timing Diagram of 68-Series 16-bit CPU Interface.

10.1.3. 68-Series 9-bit CPU interface

Bit Assignment

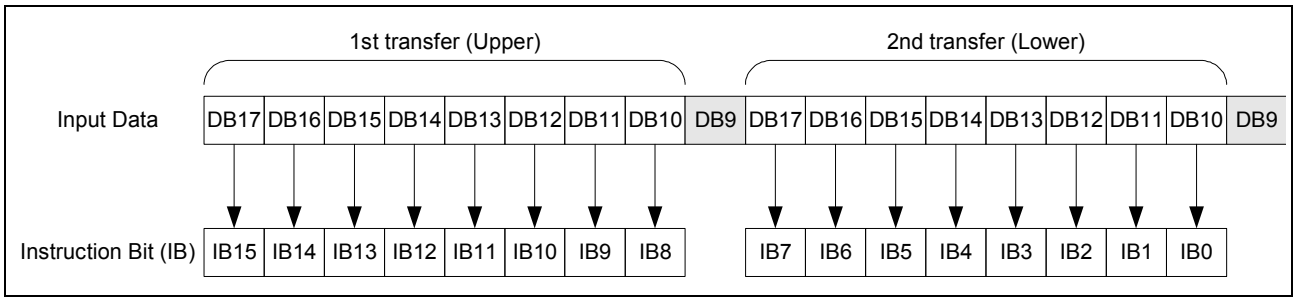


Figure 49. Bit Assignment of Instructions on 68-Series 9-bit CPU Interface.

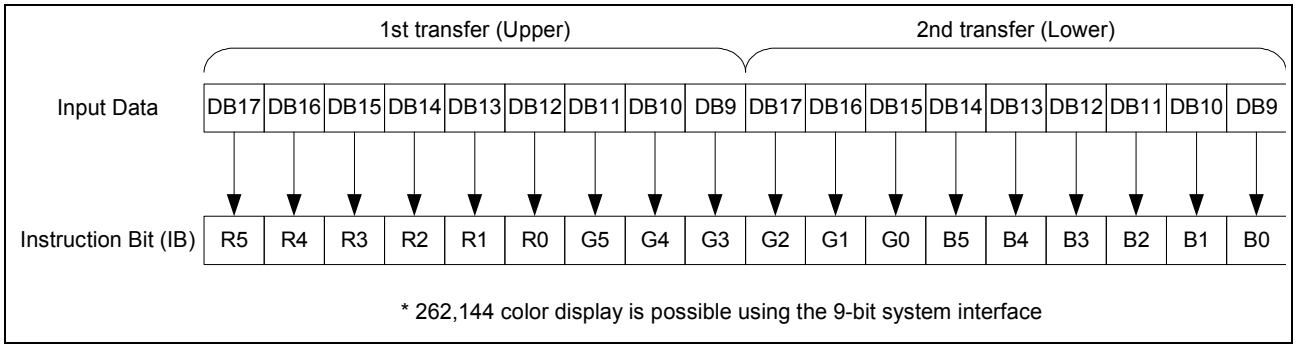


Figure 50. Bit Assignment of GRAM Data on 68-Series 9-bit CPU Interface.

Timing Diagram

There are four timing conditions for 68-Series 9-bit CPU interface: index write timing condition, data write timing condition, data read timing condition and status read timing condition. In this mode, 16-bit instructions and GRAM data are divided into two half words. The transfer starts from the upper half word.

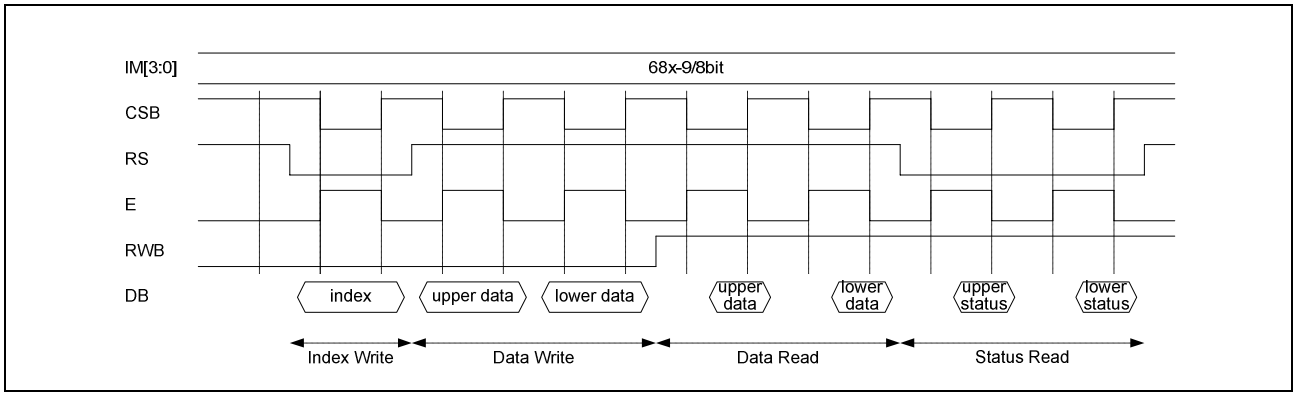


Figure 51. Timing Diagram of 68-Series 9-bit CPU Interface

10.1.4. 68-Series 8-bit CPU interface

Bit Assignment

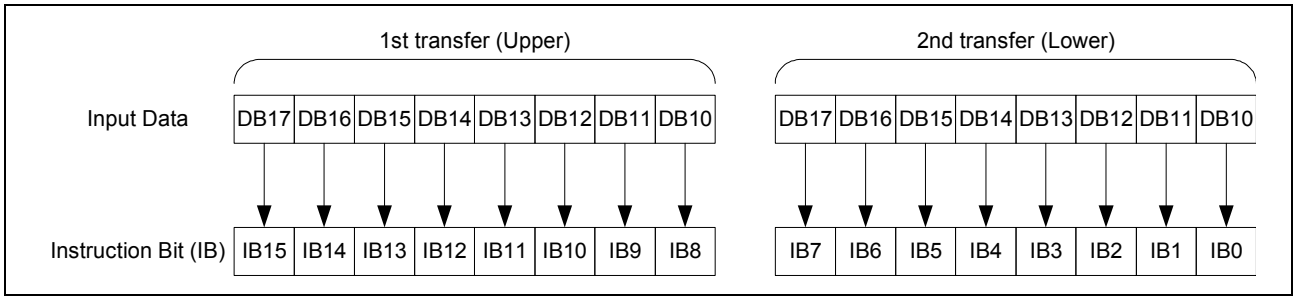


Figure 52. Bit Assignment of Instructions on 68-Series 8-bit CPU Interface

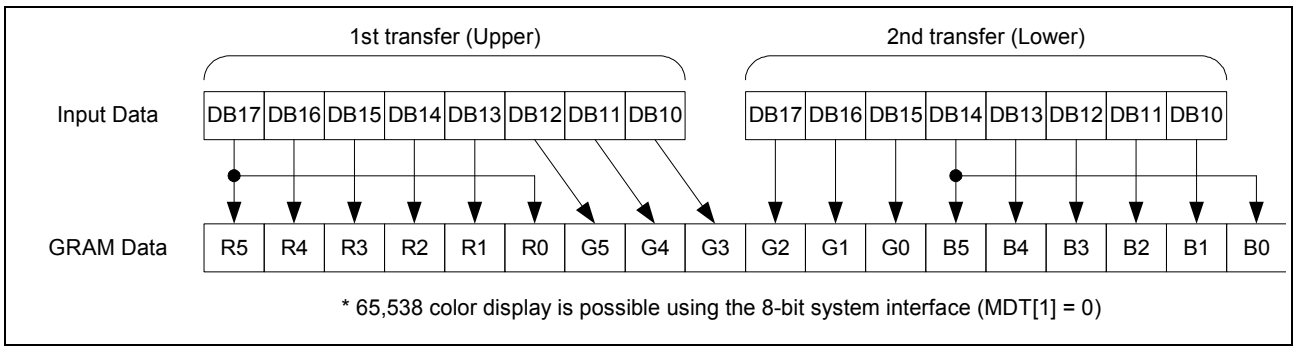


Figure 53. Bit Assignment of GRAM Data on 68-Series 8-bit CPU Interface

Timing Diagram

There are four timing conditions for 68-Series 8-bit CPU interface: index write timing condition, data write timing condition, data read timing condition and status read timing condition. In this mode, 16-bit instructions and GRAM data are divided into two half word. The transfer starts from the upper half word.

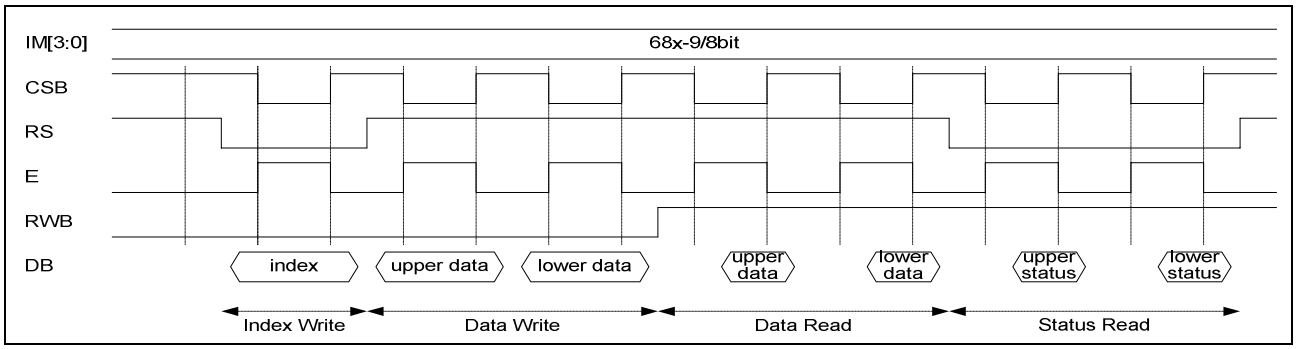


Figure 54. Timing Diagram of 68-Series 8-bit CPU Interface.

10.1.5. 80-Series 18-bit CPU interface

Bit Assignment

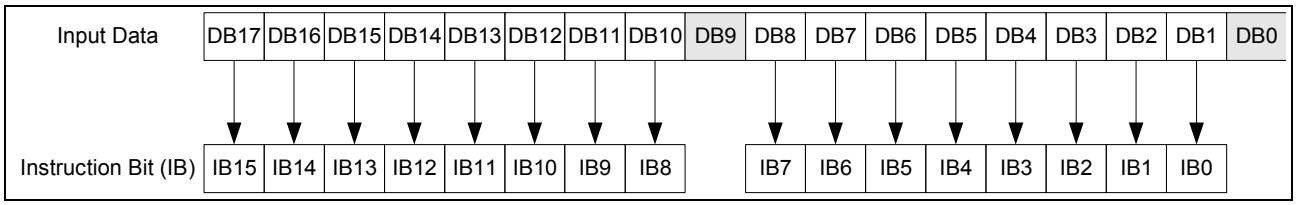


Figure 55. Bit Assignment of Instructions on 80-Series 18-bit CPU Interface.

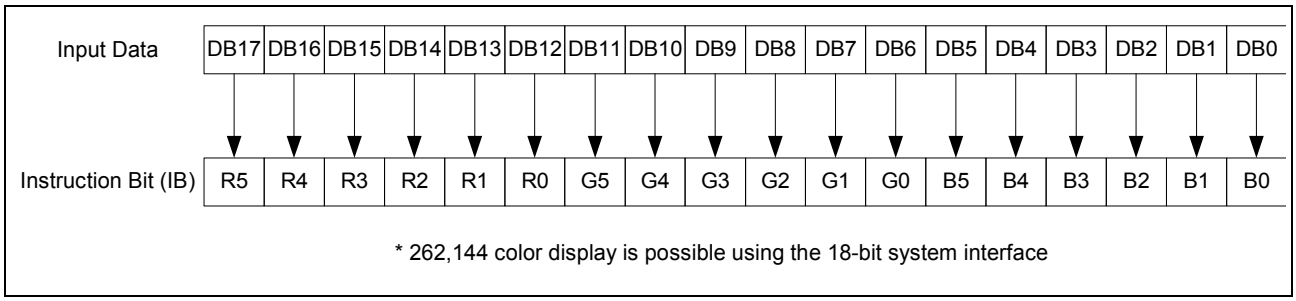


Figure 56. Bit Assignment of GRAM Data on 80-Series 18-bit CPU Interface.

Timing Diagram

There are four timing conditions for 80-Series 18-bit CPU interface: index write timing condition, data write timing condition, data read timing condition and status read timing condition.

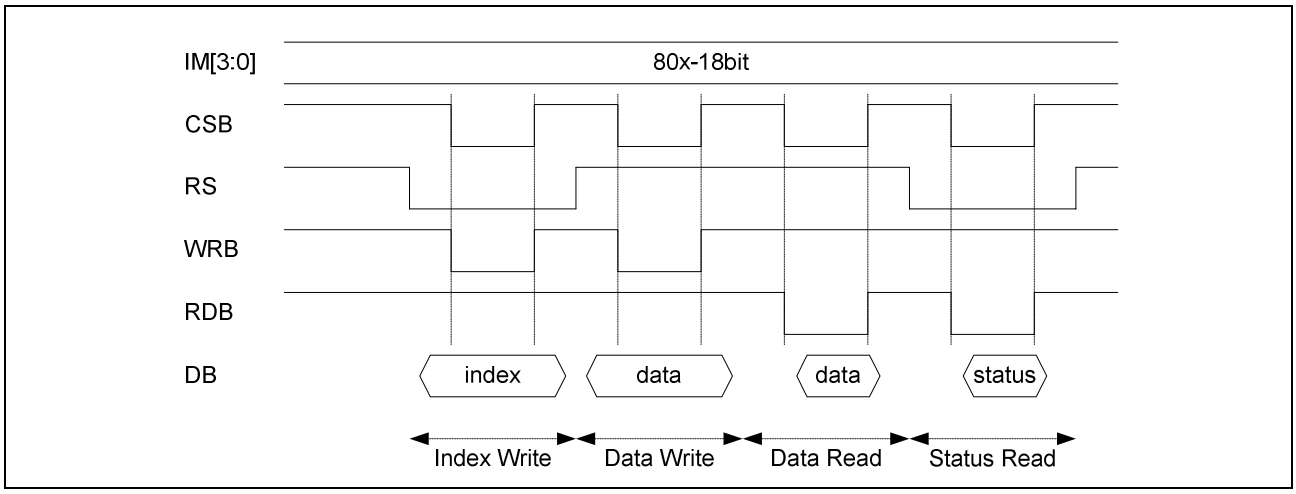


Figure 57. Timing Diagram of 80-Series 18-bit CPU Interface.

10.1.6. 80-Series 16-bit CPU interface

Bit Assignment

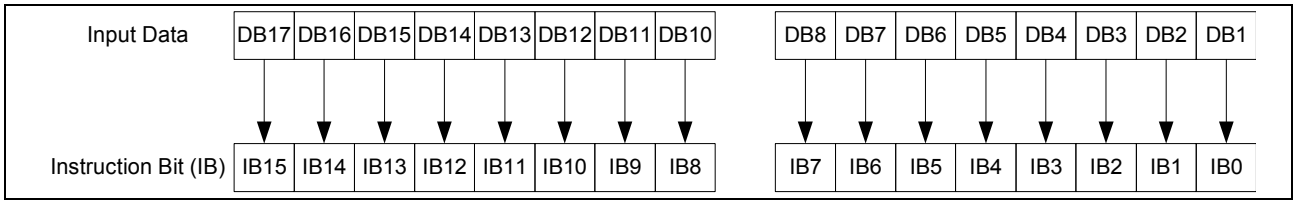


Figure 58. Bit Assignment of Instructions on 80-Series 16-bit CPU Interface.

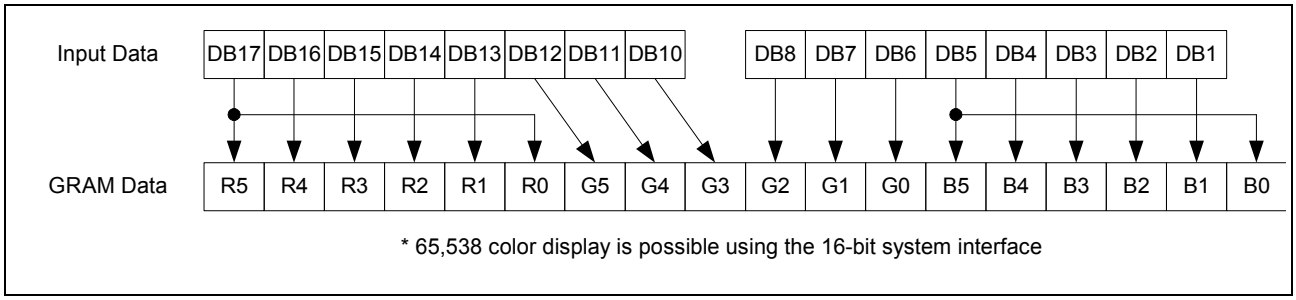


Figure 59. Bit Assignment of GRAM Data on 80-Series 16-bit CPU Interface.

Timing Diagram

There are four timing conditions for 80-Series 16-bit CPU interface: index write timing condition, data write timing condition, data read timing condition and status read timing condition.

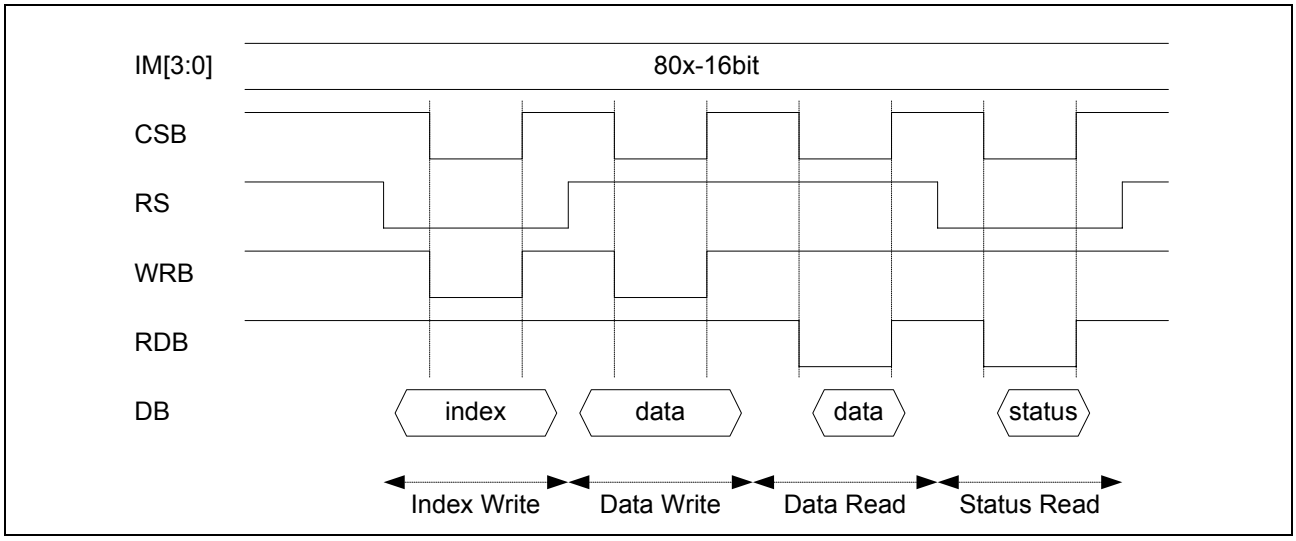


Figure 60. Timing Diagram of 80-Series 16-bit CPU Interface.

10.1.7. 80-Series 9-bit CPU interface

Bit Assignment

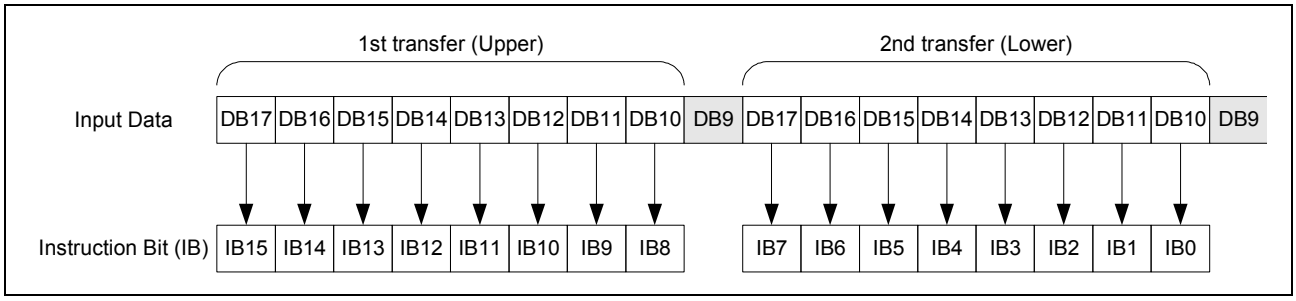


Figure 61. Bit Assignment of Instructions on 80-Series 9-bit CPU Interface.

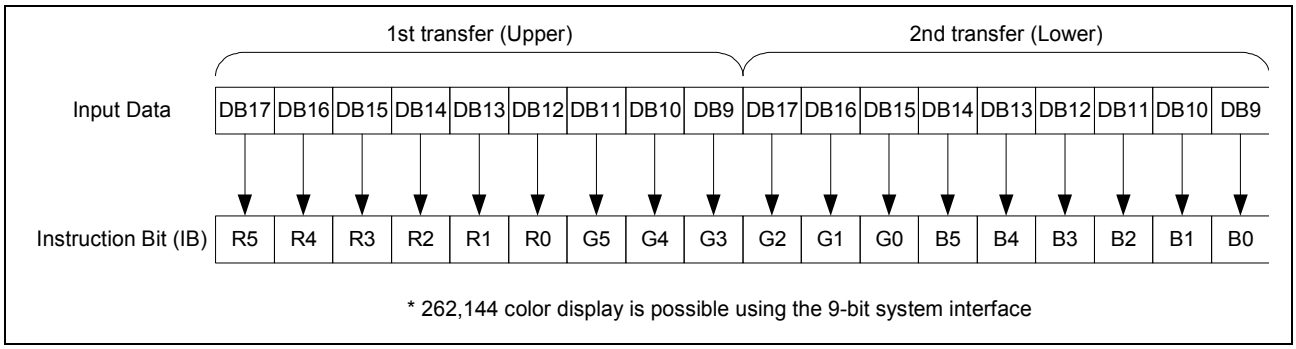


Figure 62. Bit Assignment of GRAM Data on 80-Series 9-bit CPU Interface.

Timing Diagram

There are four timing conditions for 80-Series 9-bit CPU interface: index write timing condition, data write timing condition, data read timing condition and status read timing condition. In this mode, 16-bit instructions and GRAM data are divided into two half words. The transfer starts from the upper half word.

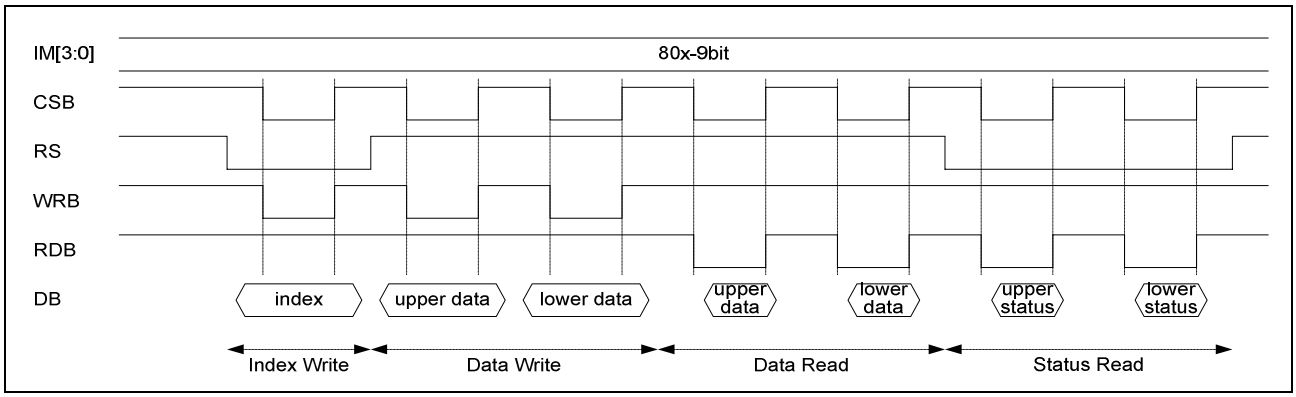


Figure 63. Timing Diagram of 80-Series 9-bit CPU Interface.

10.1.8. 80-Series 8-bit CPU interface

Bit Assignment

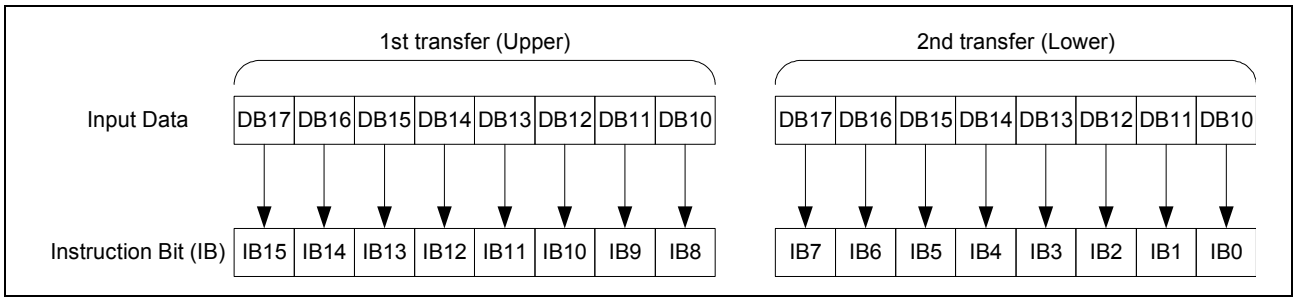


Figure 64. Bit Assignment of Instructions on 80-Series 8-bit CPU Interface.

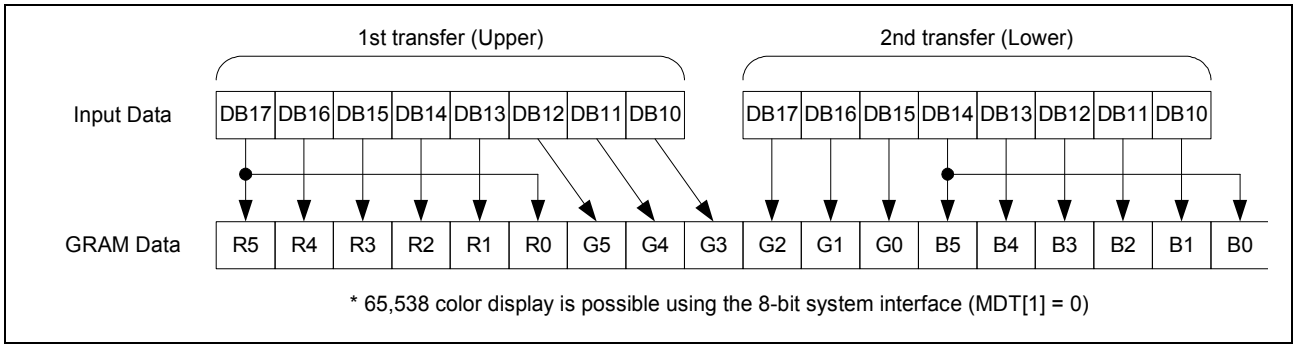


Figure 65. Bit Assignment of GRAM Data on 80-Series 8-bit CPU Interface.

Timing Diagram

There are four timing conditions for 80-Series 8-bit CPU interface: index write timing condition, data write timing condition, data read timing condition and status read timing condition. In this mode, 16-bit instructions and GRAM data are divided into two half words. The transfer starts from the upper half word.

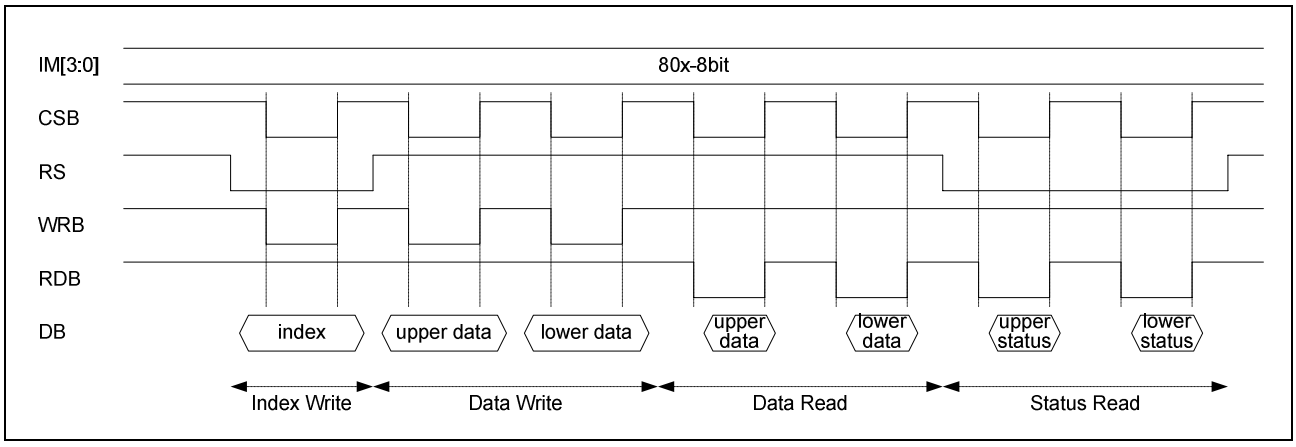


Figure 66. Timing Diagram of 80-Series 8-bit CPU Interface.

10.1.9. Serial Peripheral Interface

A clock-synchronized serial data transfer is initiated after IM[3:0] register is loaded with the data transfer command. Following signals are used for data transfers per SPI (Serial Peripheral Interface): CSB (chip select), SCL (serial transfer clock), SDI (serial input data) and SDO (serial output data). For the serial interface, IM[0] is used as an ID bit.

If IM[3:0] is loaded with 4'b0111, a 3-wire SPI mode serial data transfer will be initiated. Following pads are used in the transfer: CSB (chip select), RS (serial transfer clock), and DB[10] (serial input/output data). For 3-wire SPI, ID bit should be 1'b1.

The S6D0151 initiates serial data transfer by transferring the start byte at the falling edge of CSB input. It ends serial data transfer at the rising edge of CSB input.

The S6D0151 is selected when the 6-bit chip address imbedded in the start byte transferred by a transmitting device matches the 6-bit device identification code assigned to the S6D0151. ID bit is the least significant bit of the device identification code. The S6D0151, when selected, receives the subsequent data string.

Two different chip addresses must be assigned to the S6D0151 because the seventh bit of the start byte is used as a register select bit (RS): that is, when RS = 0, data can be written to the index register or status can be read, and when RS = 1, an instruction can be issued or data can be written to or read from GRAM. Read or write is determined according to the eighth bit of the start byte (R/WB bit). The data is written (receives) when the R/WB bit is 0, and is read (transmits) when the R/WB bit is 1.

After receiving the start byte, the S6D0151 receives or transmits serial data. The data is transferred with the MSB first. All S6D0151 instructions are 16 bits, so two bytes are received with the MSB first (DB15 to 0), and then the instruction is internally executed.

First five bytes of GRAM data read after the start byte are invalid. The S6D0151 starts to read correct GRAM data from the sixth byte. Likewise, it starts to read correct register/status from the second byte.

Table 74. Start Byte Format.

Transfer Bit	1st	2nd	3rd	4th	5th	6th	7th	8th
Start byte format	Device Identification code						RS	RWB
	0	1	1	1	0	ID		

[Note] The IM[0] pad is used as ID bit

Table 75. RS and RWB Bit Function.

RS bit	RWB bit	Function
0	0	Set index register
0	1	Read status
1	0	Writes instruction or RAM data
1	1	Reads instruction or RAM data

Bit Assignment

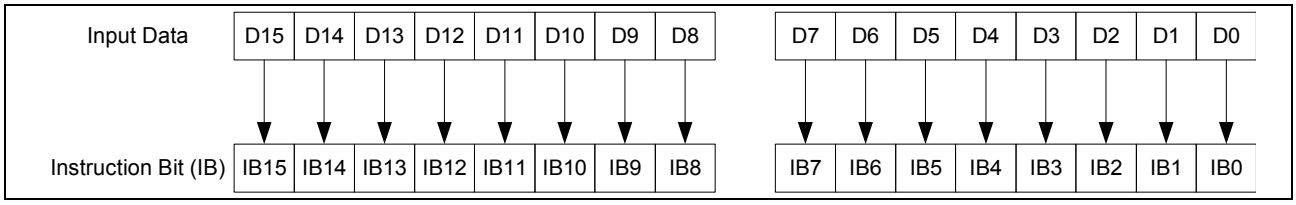


Figure 67. Bit Assignment of Instructions on SPI.

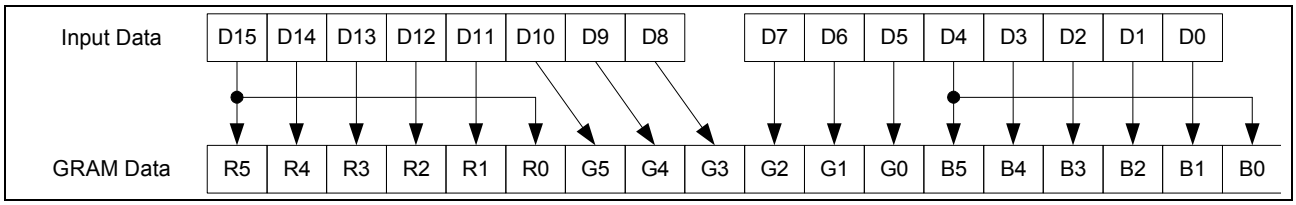


Figure 68. Bit Assignment of GRAM Data on SPI.

Timing Diagrams (IM = 4'b010X)

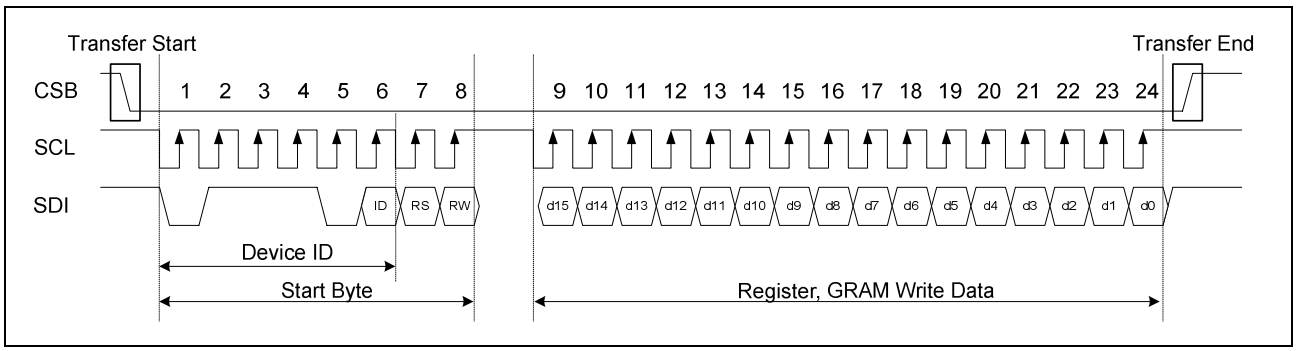


Figure 69. Typical Timing Diagram of Data Transfer through SPI (IM=4'b010X).

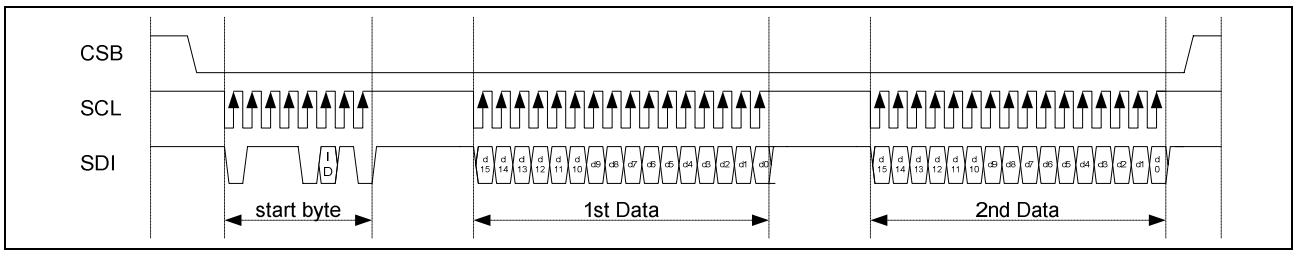


Figure 70. Timing Diagram of Consecutive Data-Write through SPI (IM=4'b010X).

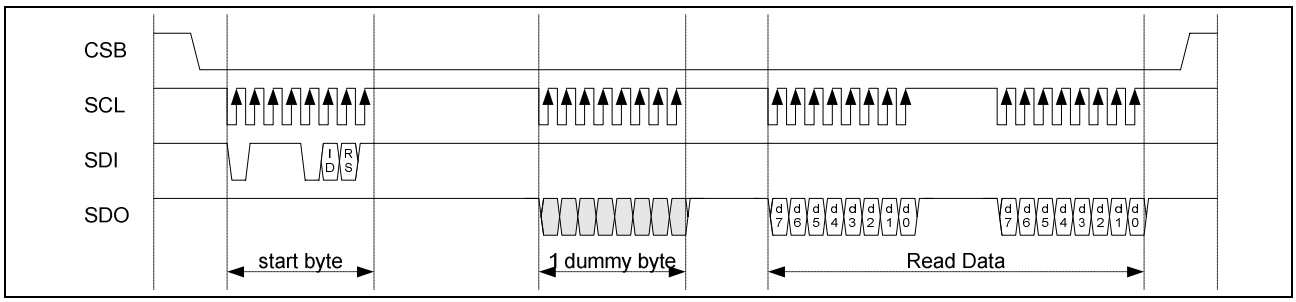


Figure 71. Timing Diagram of Register / Status Read through SPI (IM=4'b010X).

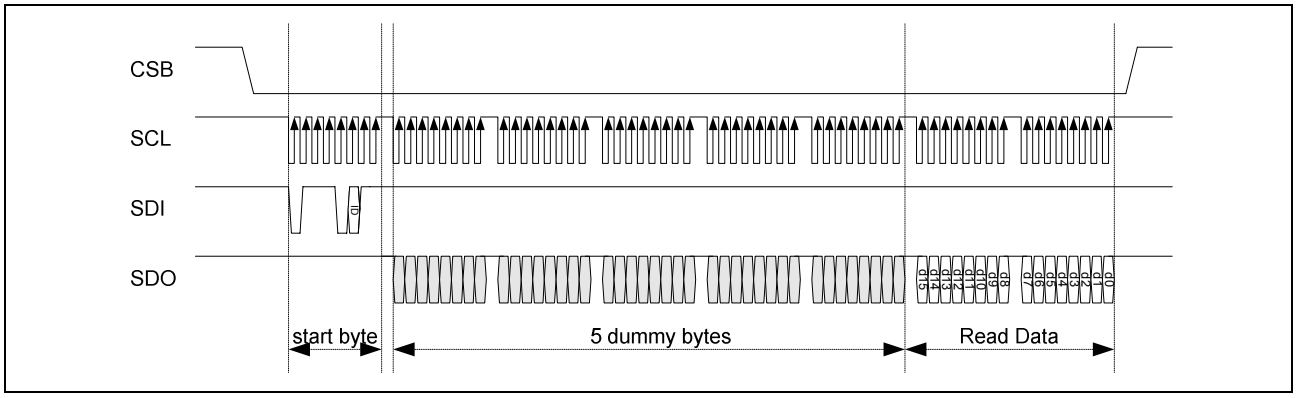


Figure 72. Timing Diagram of GRAM-Data Read through SPI (IM=4'b010X).

Timing Diagrams (IM = 4'b0111)

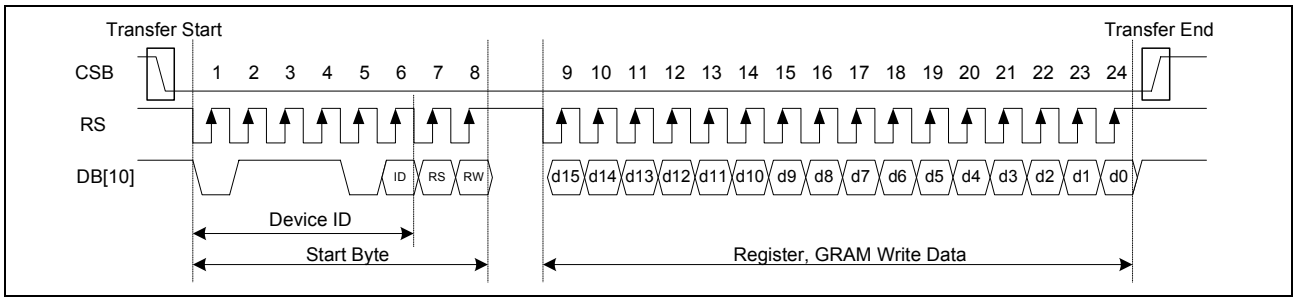


Figure 73. Basic Timing Diagram of Data Transfer through SPI (IM=4'b0111).

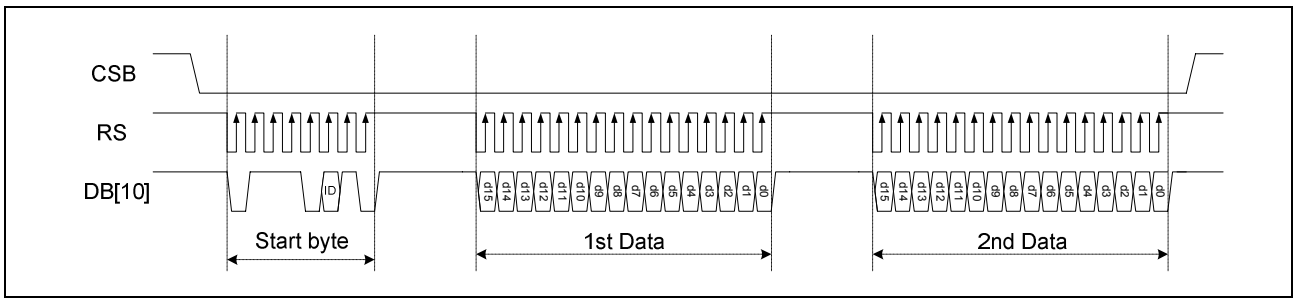


Figure 74. Timing Diagram of Consecutive Data-Write through SPI (IM=4'b0111).

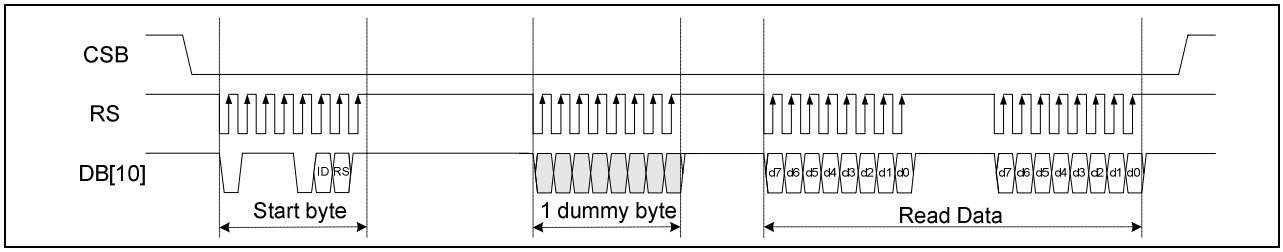


Figure 75. Timing Diagram of Register / Status Read through SPI (IM=4'b0111).

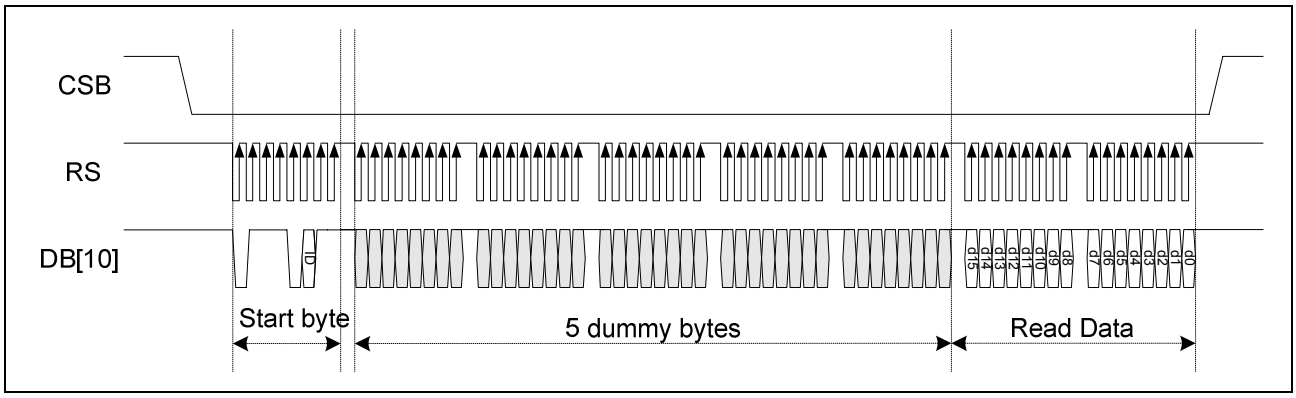


Figure 76. Timing Diagram of GRAM-Data Read through SPI (IM=4'b0111).

10.2. RGB interface

10.2.1. Motion picture display

The S6D0151 incorporates RGB interface to display motion pictures and GRAM to display still pictures. For displaying motion pictures, it utilizes following features:

- Only motion picture area can be transferred by the Window Address function.
- Only motion picture area to be rewritten can be transferred selectively.
- Reducing the amount of data transferred reduces overall power consumption.
- Still picture area, such as an icon, can be updated while displaying motion pictures (for details, refer to GRAM Access Via RGB Interface and SPI section described later).

The RGB interface is performed in synchronization with VSYNC, HSYNC, and DOTCLK.
Window Address Function facilitates in transferring data corresponding to the portion of screen to be updated, hence, reducing the overall power consumption.

In the period between the completion of displaying one frame data and the next VSYNC signal, the display status will remain in front porch.

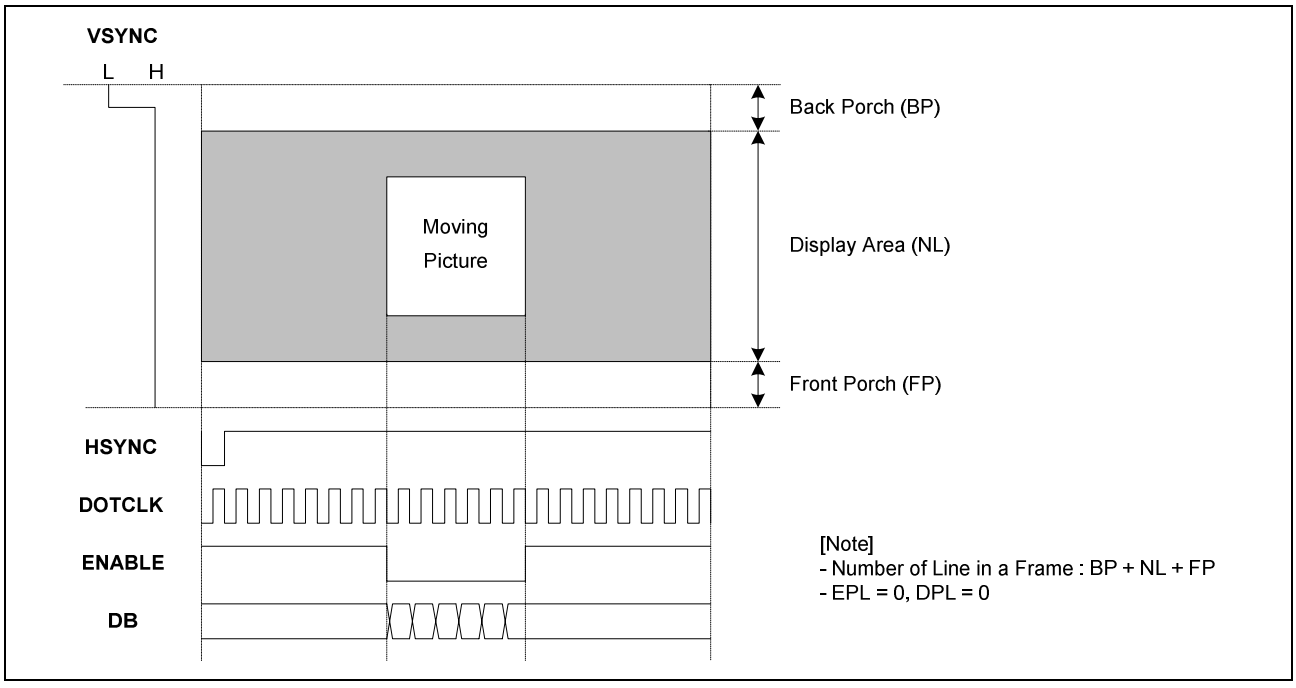


Figure 77. RGB Interface.

[Note] For RGB interface, VSYNC, HSYNC, DOTCLK should be supplied at much higher resolution than that of panel.

There are three timing conditions for RGB Interface that is determined according to RIM and each condition is described below.

10.2.2. 18-bit RGB interface

Bit Assignment

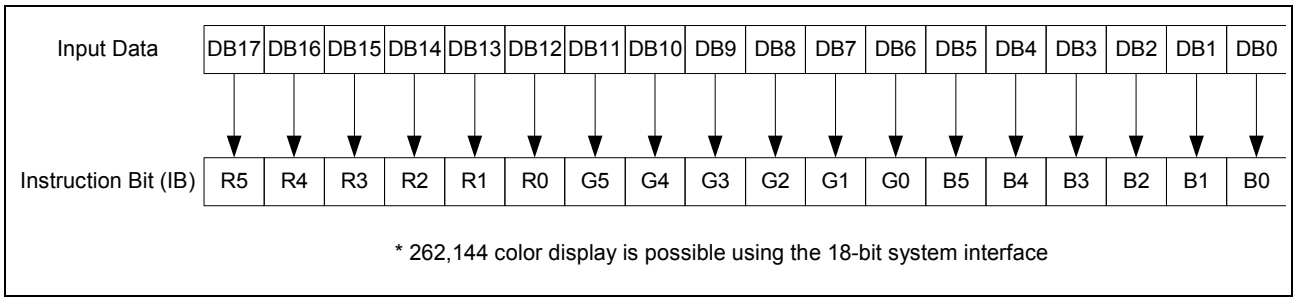


Figure 78. Bit Assignment of GRAM Data on 18-bit RGB Interface.

Timing Diagram

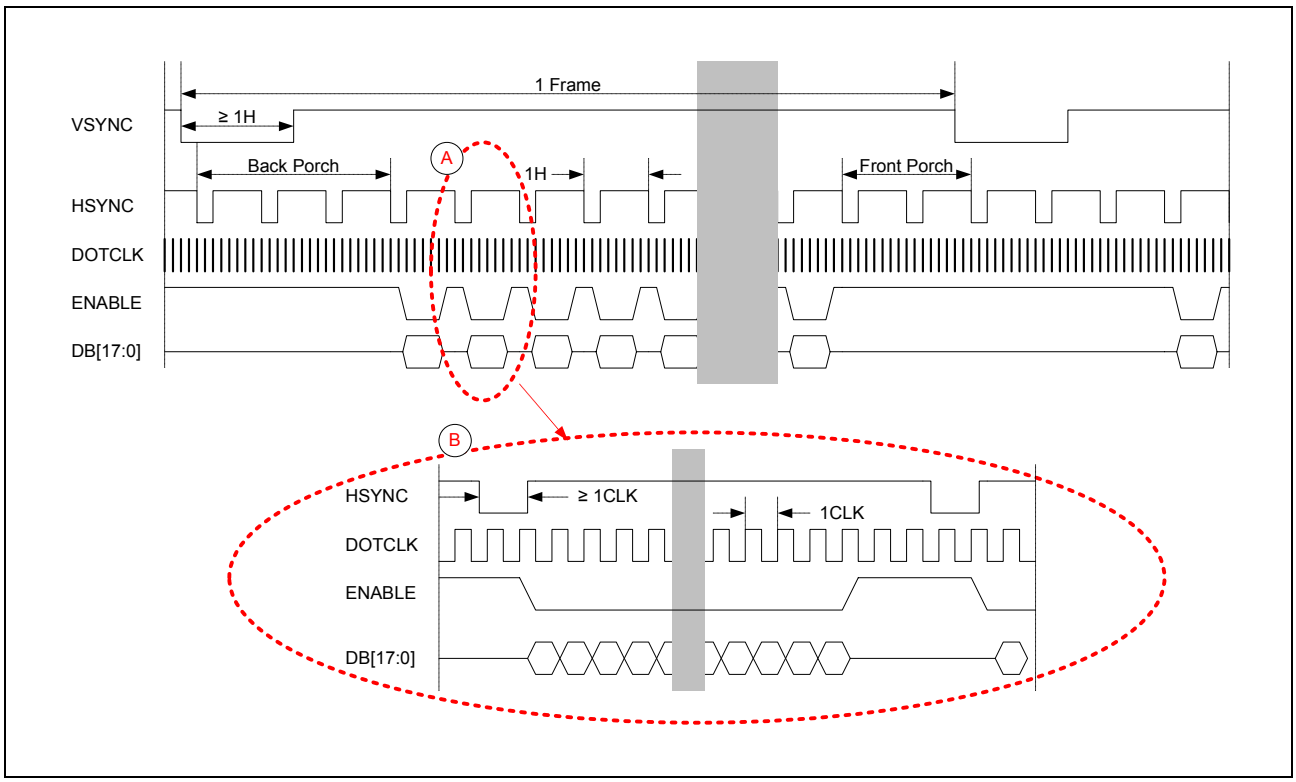


Figure 79. Timing Diagram of 18/16bit RGB Interface.

10.2.3. 16-bit RGB interface

Bit Assignment

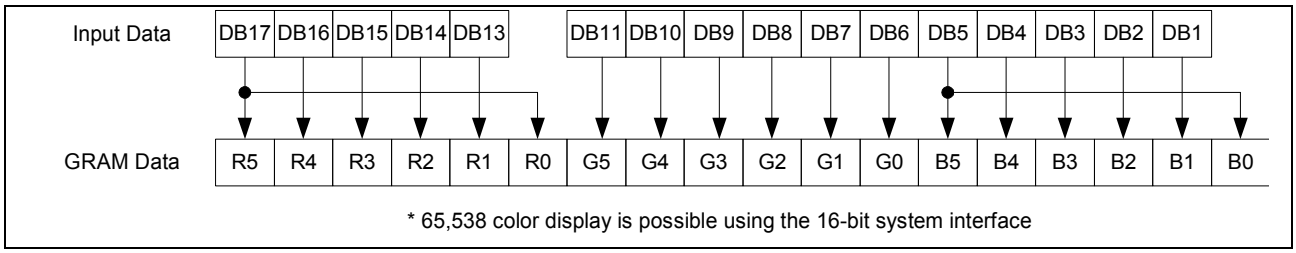


Figure 80. Bit Assignment of GRAM Data on 16bit RGB Interface.

Timing Diagram

There are two timing conditions for RGB Interface that is determined according to RIM.

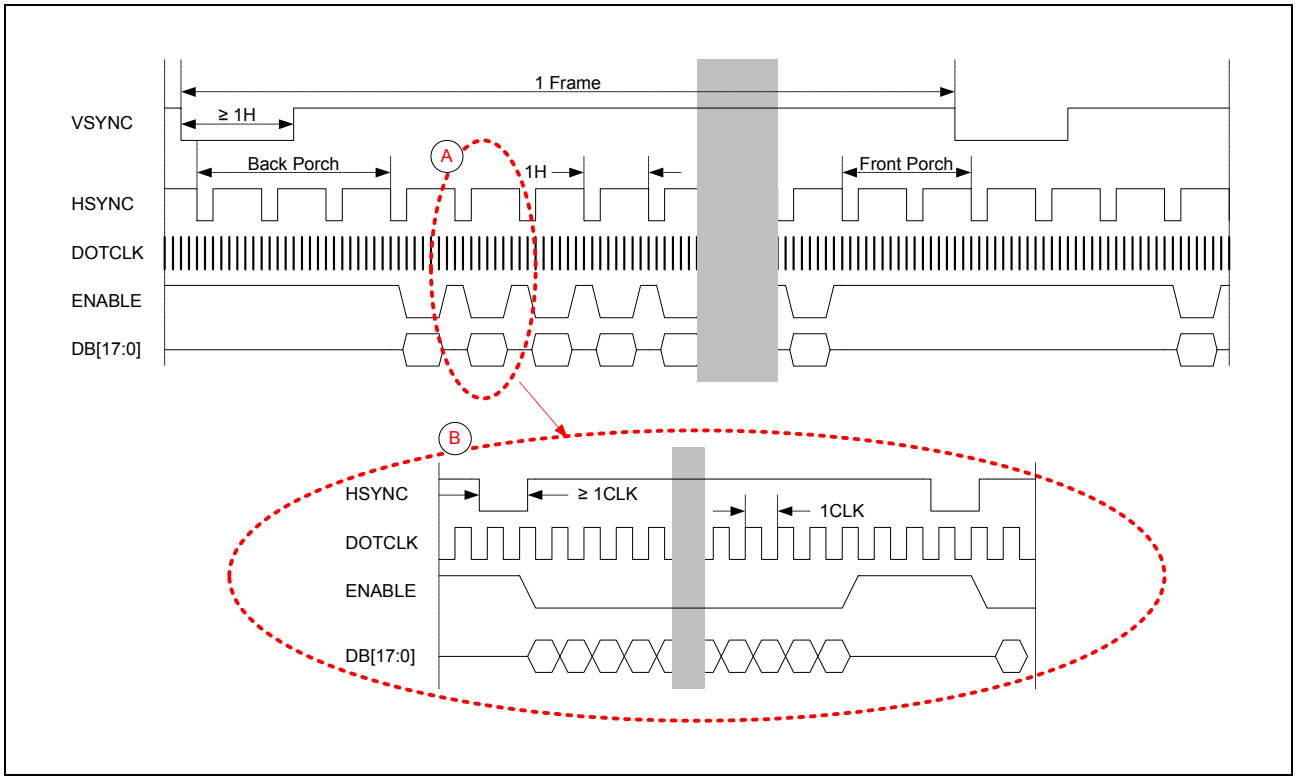


Figure 81. Timing Diagram of 18/16bit RGB Interface.

10.2.4. 6-bit RGB interface

In order to transfer data on 6bit RGB Interface there should be three transfers.

Bit Assignment

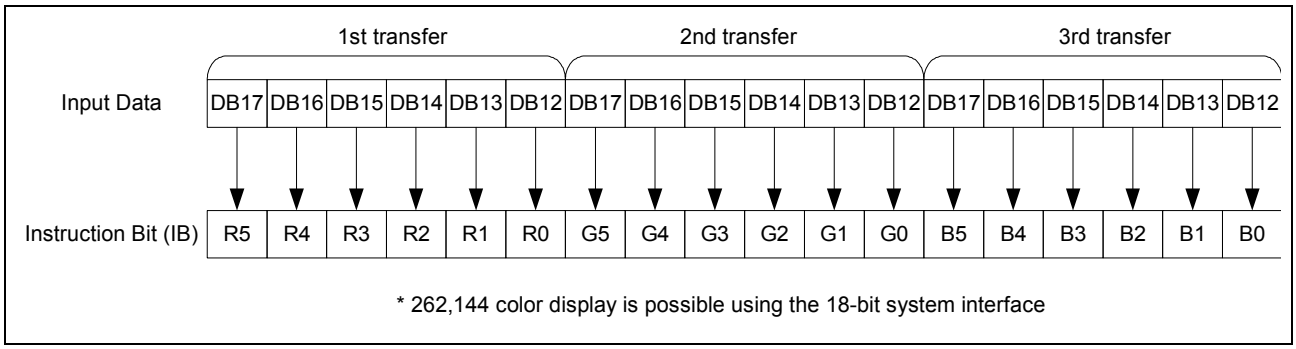


Figure 82. Bit Assignment of GRAM Data on 6bit RGB Interface.

Timing Diagram

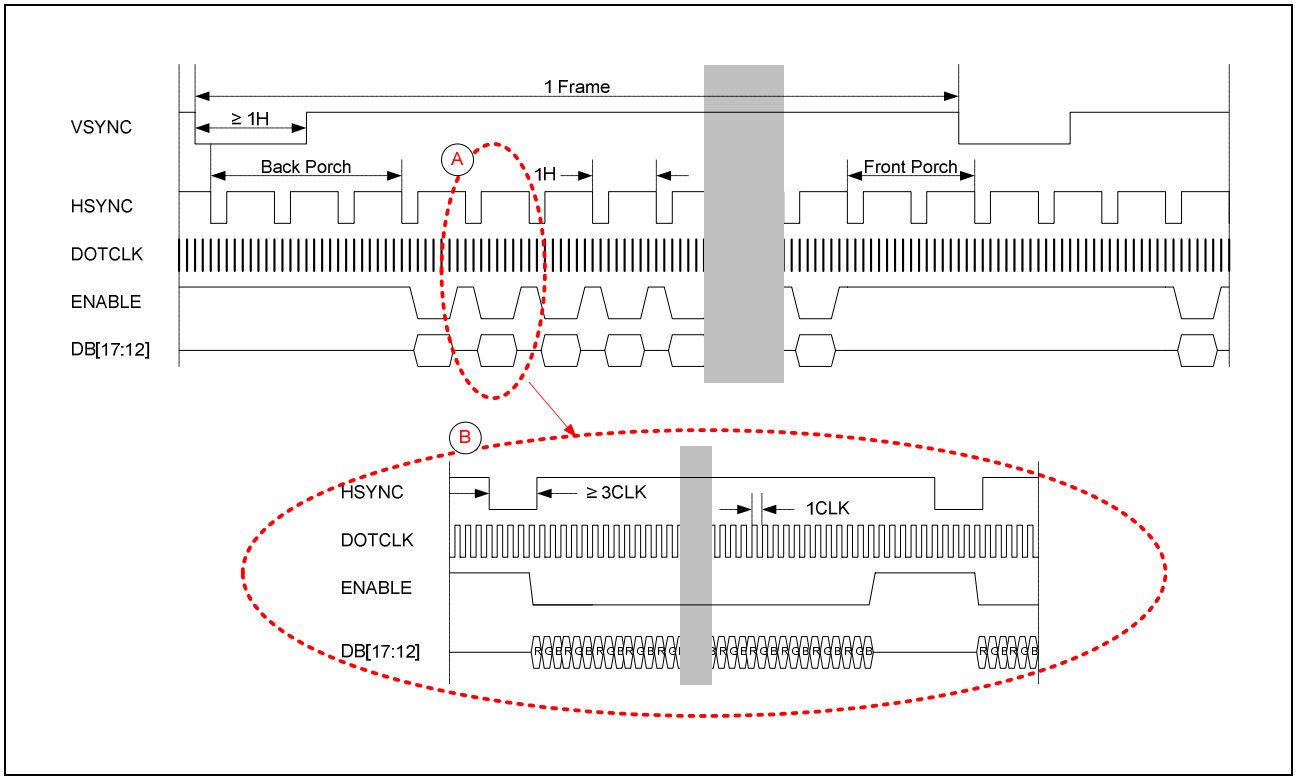


Figure 83. Timing Diagram of 6bit RGB Interface.

[Note]

1. Three clocks are regarded as one clock for transfer when data is transferred in 6-bit interface.

2. VSYNC, HSYNC, ENABLE, DOTCLK, and DB[17:12] should be transferred in units of three clocks.

Transfer Synchronization

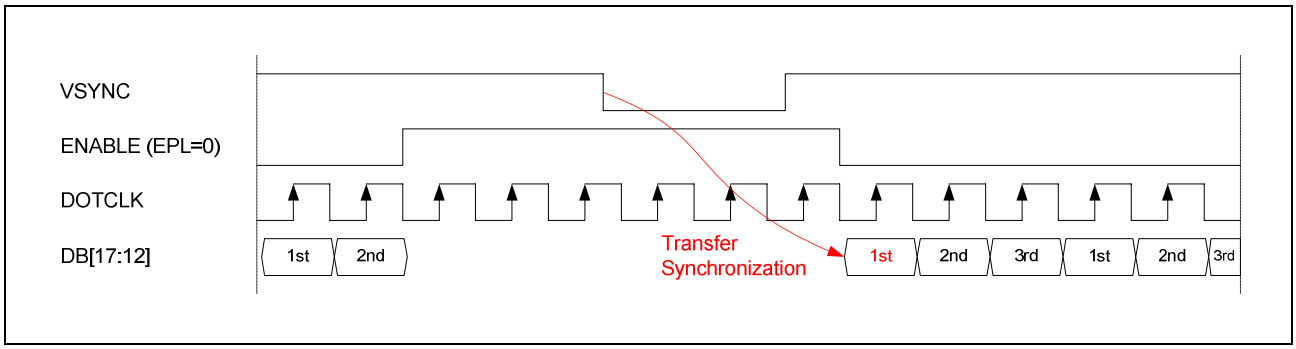


Figure 84. Transfer Synchronization Function in 6-bit RGB Interface mode.

[Note]

1. The figure above shows Transfer Synchronization function for 6-it RGB Interface. The S6D0151 has a transfer counter internally to count 1st, 2nd and 3rd data transfer of 6bit RGB Interface. The transfer counter is reset on the falling edge of VSYNC and enters the 1st data transmission state. Transfer mismatch can be corrected at every VSYNC signal assertion. In this method, when data is consecutively transferred in for displaying motion pictures, the effect of reduced and recovered transmission error is minimized and quickly recovered by normal operation.

2. The internal display is operated in units of three DOTCLKs. When DOTCLK is not inputted in units of pixels, clock mismatch occurs and the frame, which is operated, and the next frame is not displayed correctly.

10.3. Interface swapping for Memory access

10.3.1. Display modes and GRAM access control

Display mode and RAM Access is controlled as shown below. For each display status, display mode and RAM Access controls need to be set appropriately as shown in Table 73.

Table 76. Display mode & RAM access control.

Display Status	GRAM Access (RM)	Display Mode (DM)
1. Still Picture Display	System Interface (RM = 0)	Internal Clock Operation (DM[1:0] = 00)
2. Motion Picture Display	RGB Interface (RM = 1)	External Clock Operation (DM[1:0] = 01)
3. Rewrite Still Picture while Motion Picture is being displayed	System Interface (RM = 0)	External Clock Operation (DM[1:0] = 01)

[Note]

1. Only system interface can set Instruction register.

2. Do not change the RGB Interface mode (RIM) in the middle of an operation.

Internal Clock Operation mode with System Interface (1)

Every operation in Internal Clock Operation mode is done in synchronous with the internal clock which is generated by internal OSC. In this mode, any data asserted on the RGB interface will be ignored. Access to internal GRAM is done via system interface.

External Clock Operation mode with RGB Interface (2)

In External Clock Operation mode, frame sync signal (VSYNC), line sync signal (HSYNC) and DOTCLK are used for display operation. Display data is transferred in the unit of pixel through DB bus and saved to GRAM.

External Clock Operation mode with System Interface (3)

Writes GRAM data via system interface even in External Clock Operation mode. There should not be any data transmission on RGB interface in this case. To restart data transmission on RGB interface, set RM to 1, set memory address properly and write index of 22h for GRAM write operation.

With the combination of Window Address function, motion and still pictures may be saved in separate GRAM regions respectively. In this case, motion and still pictures are displayed simultaneously.

10.3.2. GRAM access via RGB interface and SPI

All the data for display is written to the internal GRAM in the S6D0151 when RGB interface is in use. In this method, data, including motion picture and screen update frame, can only be transferred via RGB interface.

With Window Address function, power consumption can be reduced and high-speed access can be achieved while motion pictures are being displayed. Data for display that is not in the motion picture area or the screen update frame can be written via System Interface.

GRAM can be accessed via SPI even when RGB interface is in use. To do that ENABLE should be in inactive state to stop data writing via RGB interface, because the write operation to GRAM is always performed in synchronous with DOTCLK while ENABLE is in active state. Then any data may be written through SPI. After this access to GRAM via SPI, a waiting time is needed for a write/read bus cycle before the next RAM access starts via RGB interface. When a RAM write conflict occurs, the integrity of write operation is not guaranteed.

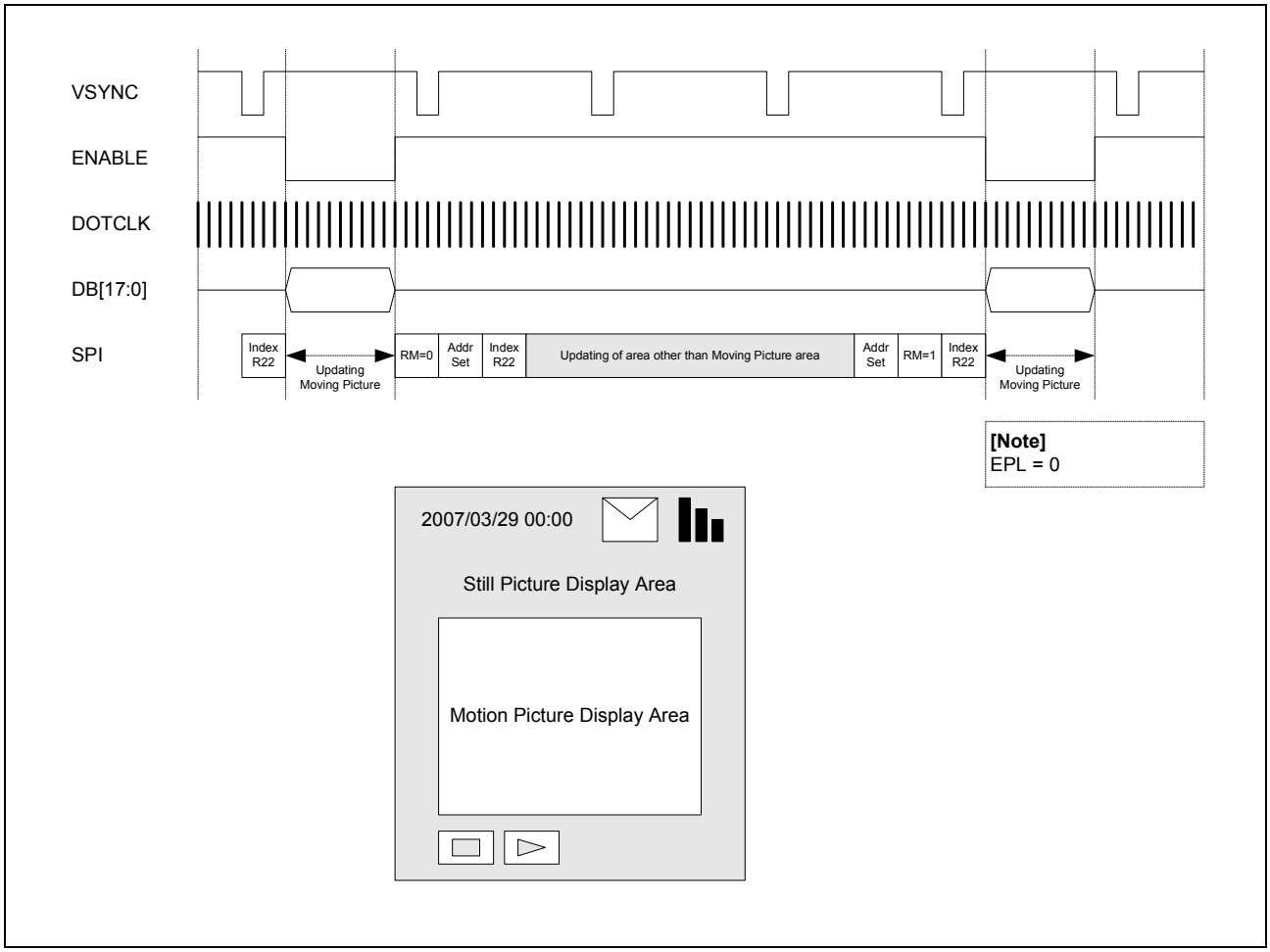


Figure 85. GRAM Access through RGB Interface and SPI.

10.3.3. Transition sequence between display modes

Transitions between Internal Clock Operation mode and External Clock Operation mode should follow the mode transition sequence shown below.

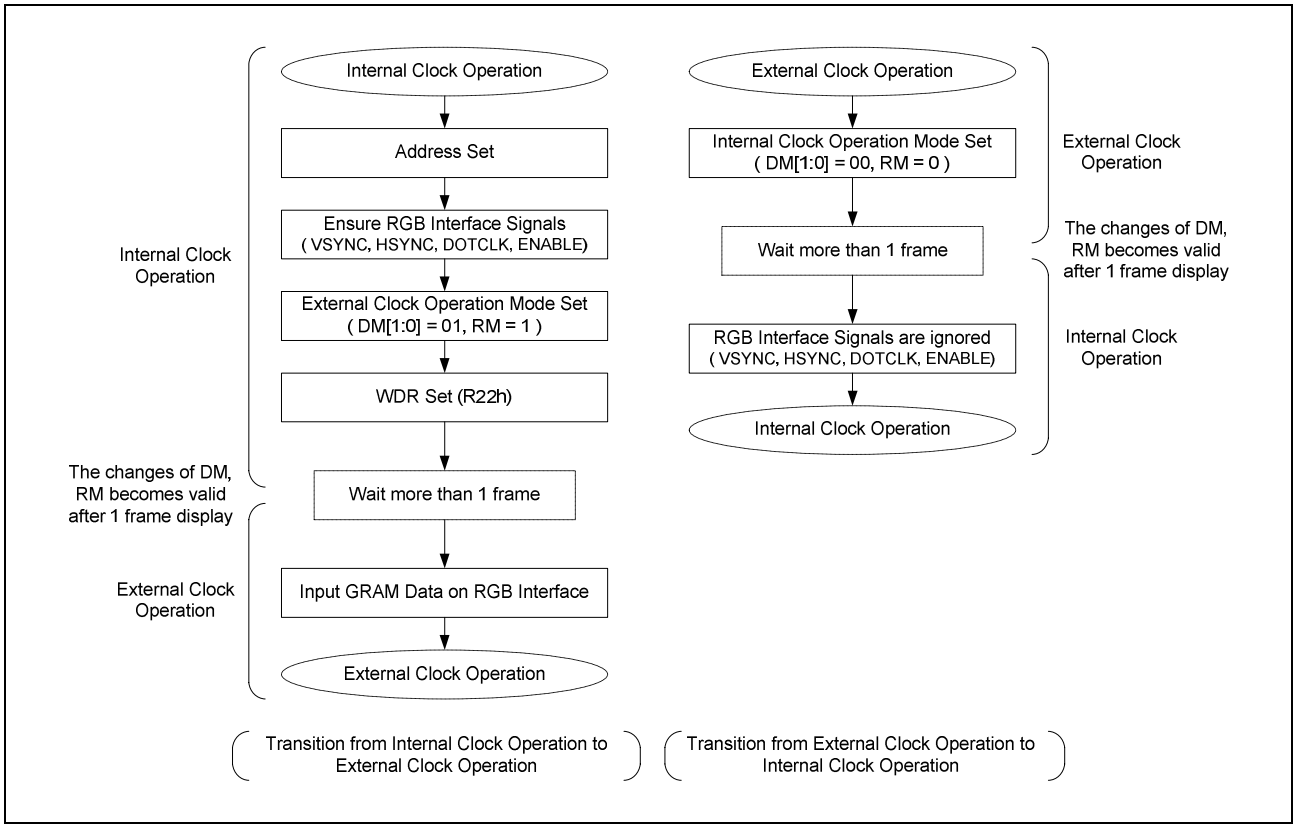


Figure 86. Transition between Internal Clock Operation Mode and External Clock Operation Mode.

10.4. Panel Control interface

10.4.1. Interconnection between panel and the IC

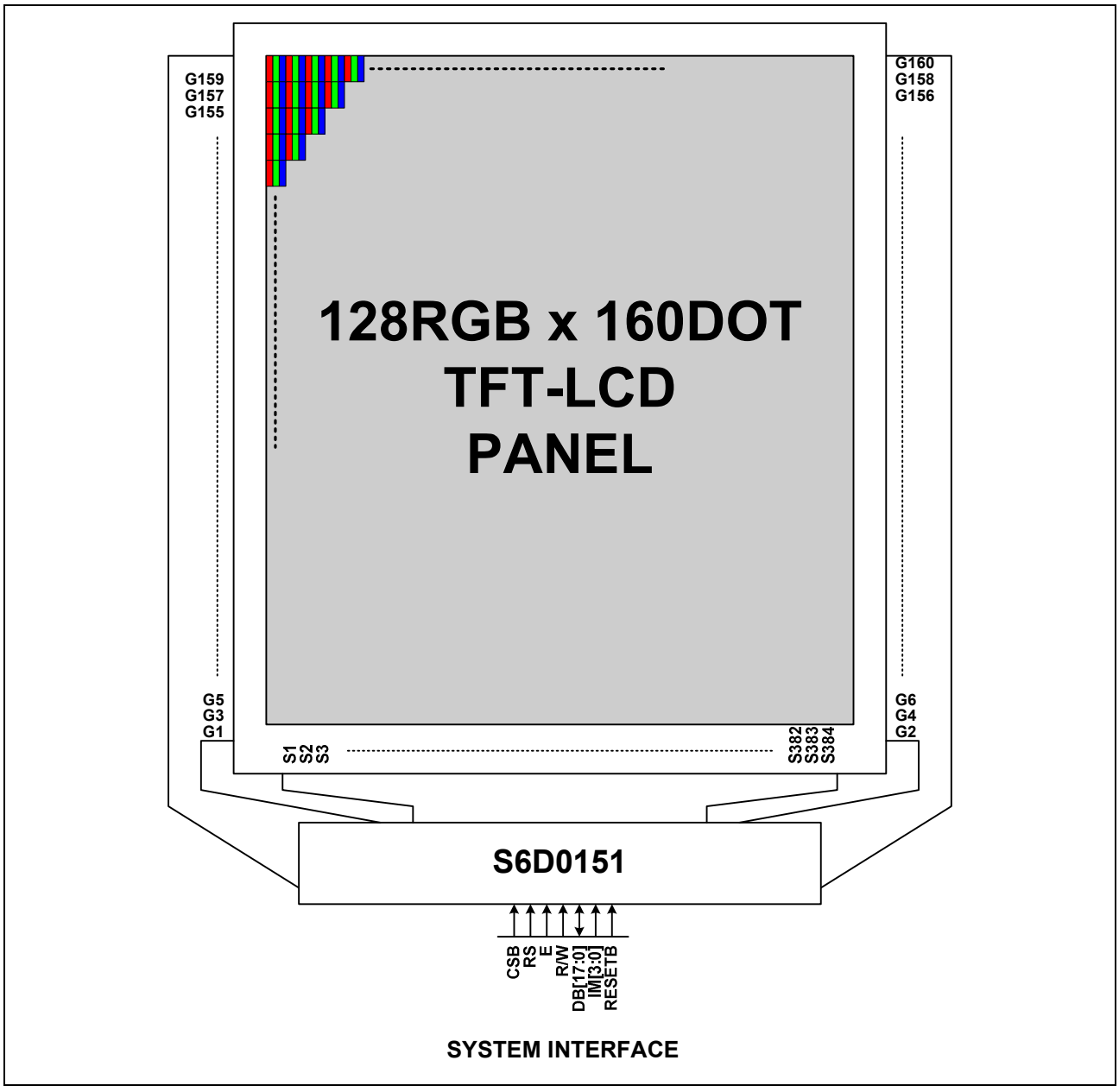


Figure 87. System structure.

10.5. Timing diagrams

Frame Inversion & Line Inversion

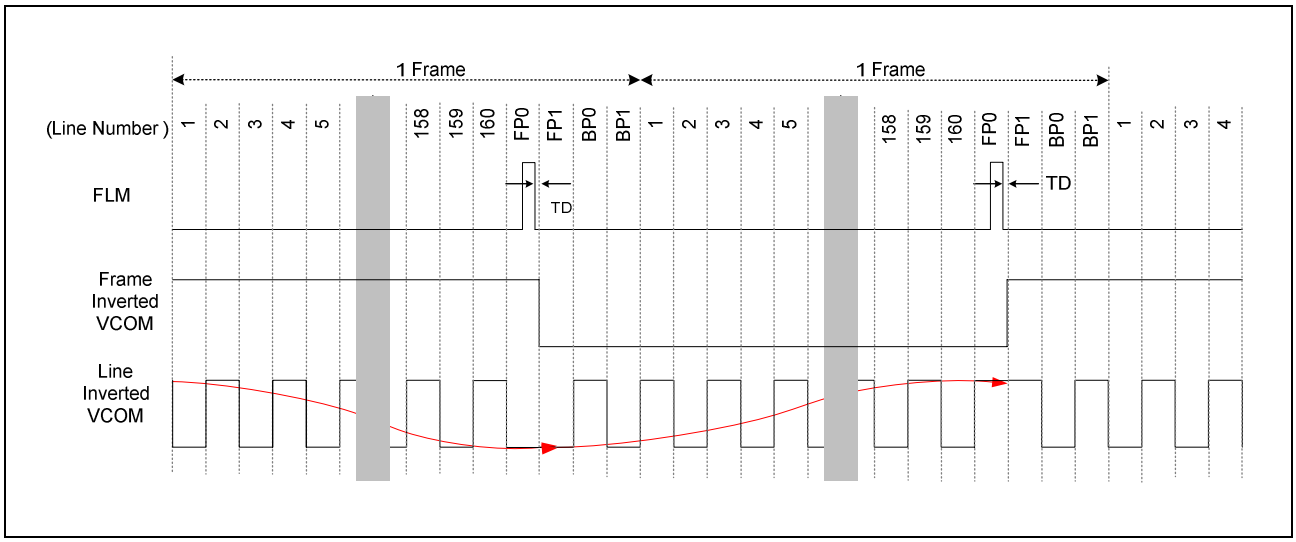


Figure 88. VCOM waveforms and LCD inversion (BP = 2, FP = 2).

[Note]

TD = 1.5DISP_CK + Gate Non-overlap period + Delay Amount of the Source Output)

- Gate Non-overlap period : defined by R71h GNO[1:0].
- Delay Amount of the Source Output : defined by R70h SDT[1:0].
- DISP_CK : OSC_CK divided by DIV[1:0](DM=2'b00) or DOTCLK divided by 8 (DM = 2'b01 and RIM[1] = 1'b1)

Example)

R70h SDT[1:0]=00, R71h GNO[1:0]=00,

TD = 1.5DISP_CK + 2DISP_CK + 1 DISP_CK = 4.5 DISP_CK

Source Output & Gate Clock

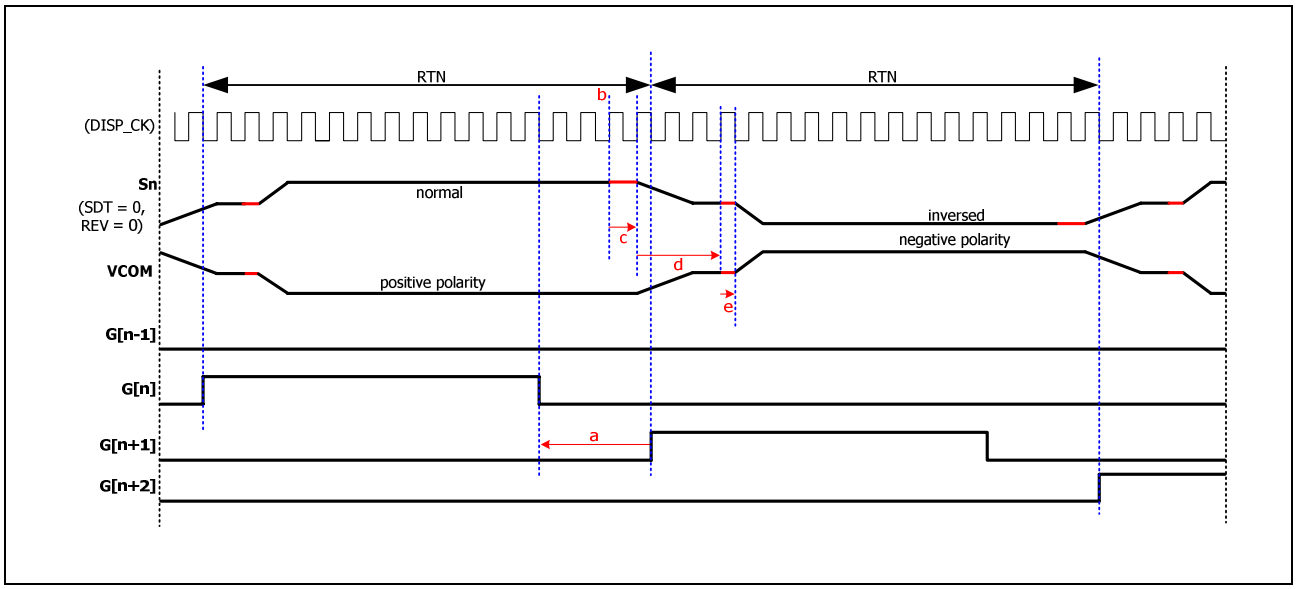


Figure 89. Source Output & Gate Clock Timing.

[Note]

Condition : EQ=2'b11, GNO=2'b01, DIV=2'b00

a = GNO, Gate Non-overlap period could adjust from the Reference point which is G[n+1] start position.

b = "b" is the start point of SDT and it placed 1.5 DISP_CK in front of G[n+1] start position.

c = SDT (Delay Amount of the Source Output) could adjust from the "b".

d = EQ, sustained for the number of clock cycle from the end of "c".

e = Floating during 0.5 DISP_CK after EQ.

DISP_CK = OSC_CK divided by DIV[1:0](DM = 2'b00) or DOTCLK divided by 8(DM = 2'b01 and RIM[1] = 1'b1)

Interlaced Scanning Function

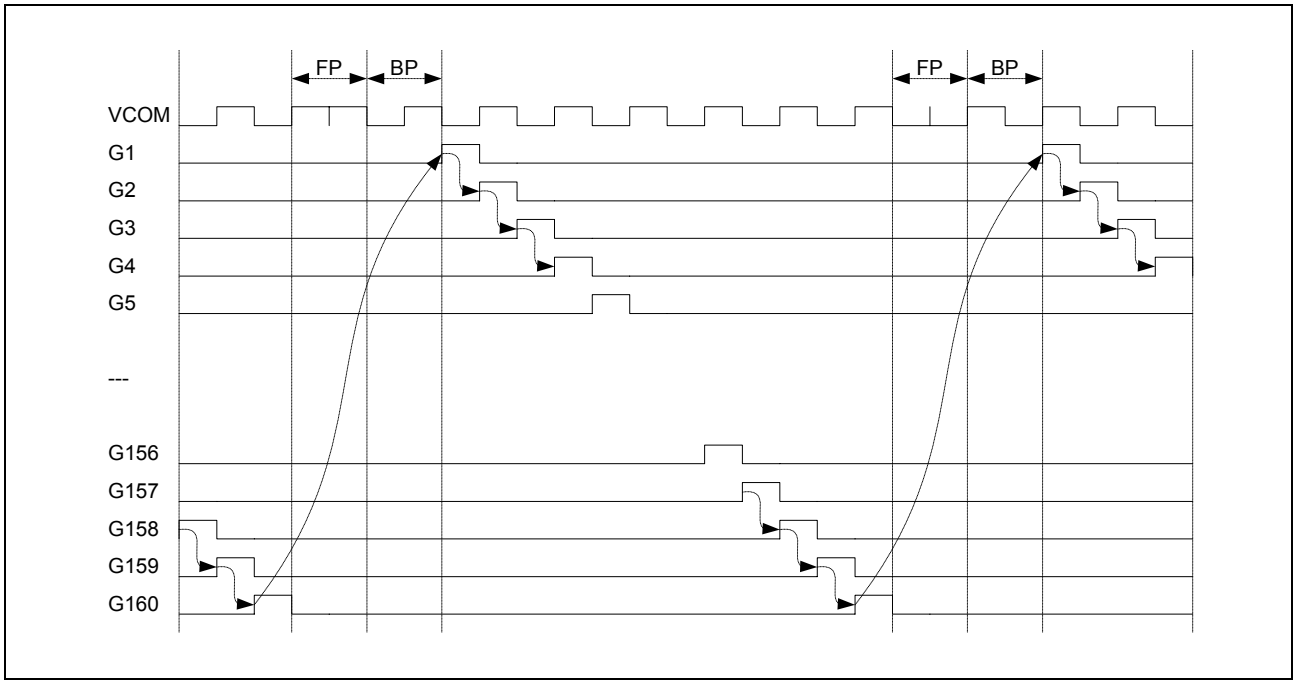


Figure 90. Normal scanning method (Line Inversion).

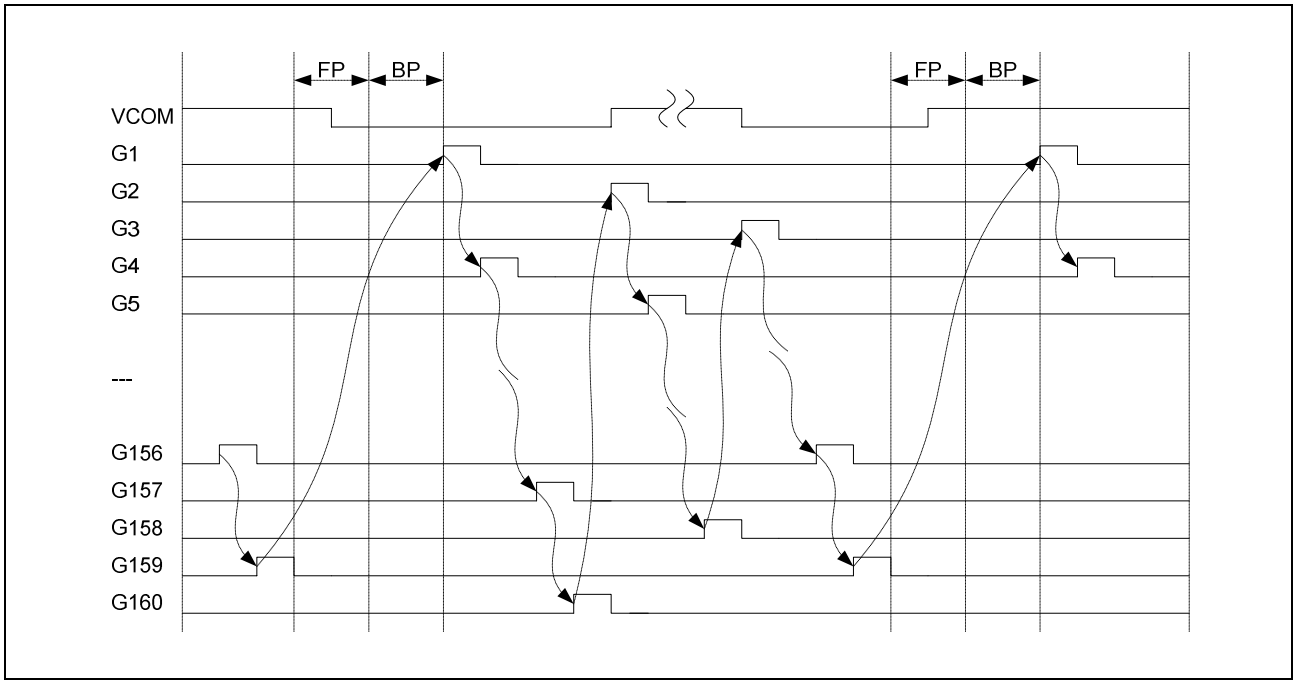


Figure 91. 3-field interlaced scanning method.

11. Gamma Adjustment Function

The S6D0151 provides gamma adjustment functionality to display 262,144 colors. This functionality is implemented with three registers that can switch the polarities of their contents: gradient adjustment register, micro-adjustment register, and amplitude adjustment register. A total of eight coarse grayscale voltages (VIN0-VIN7) are generated under the control of the aforementioned registers. The voltages are, then, fed into the grayscale amplifiers described in the following section.

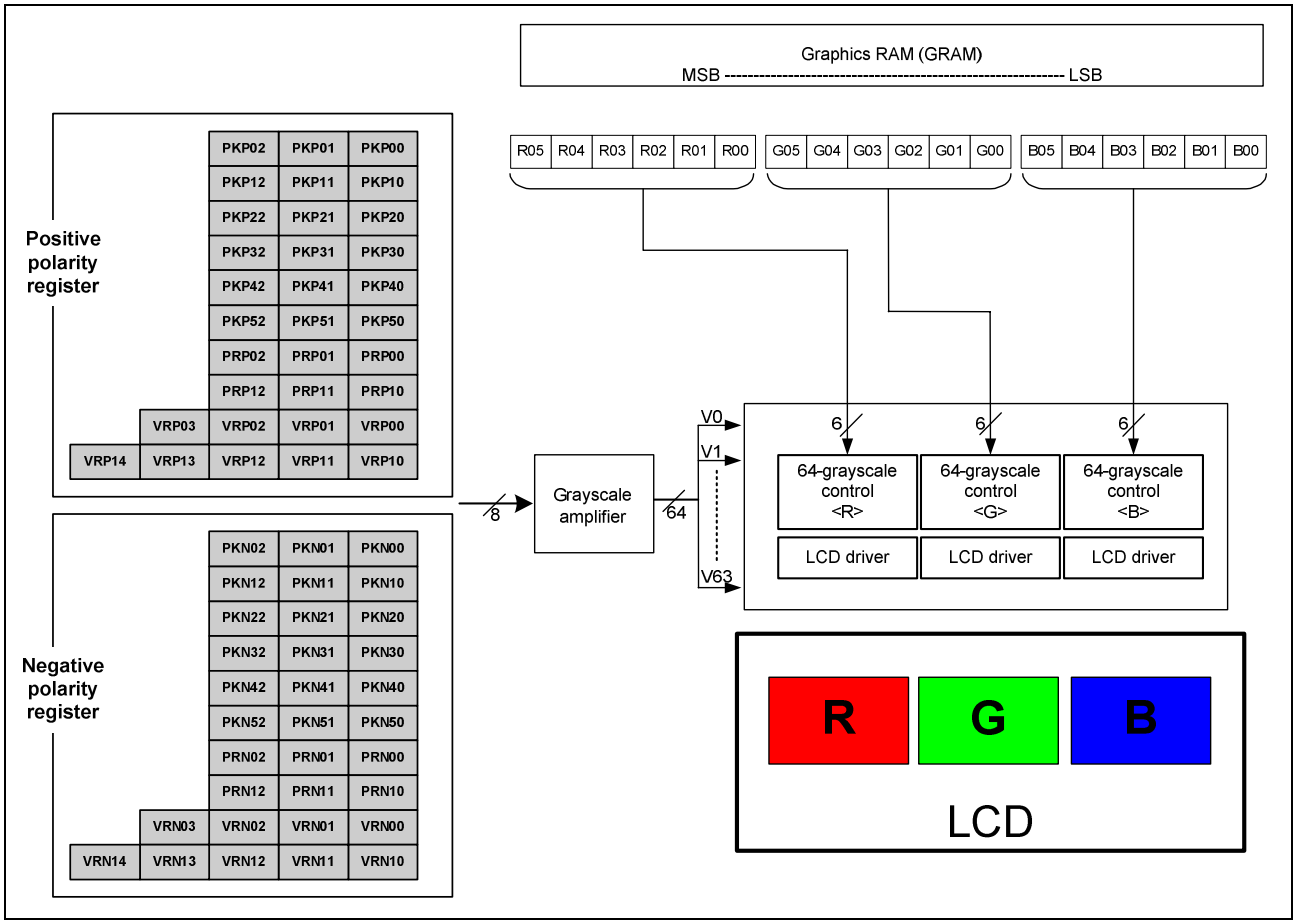


Figure 92. Grayscale control.

11.1. Structure of Grayscale amplifier

The structure of the grayscale amplifier is shown in Figure 93. The eight voltages (VIN0-VIN7) generated in the preceding section are further subdivided into 64 grayscale voltages (V0-V63) by the grayscale amplifier through internal ladder resistors.

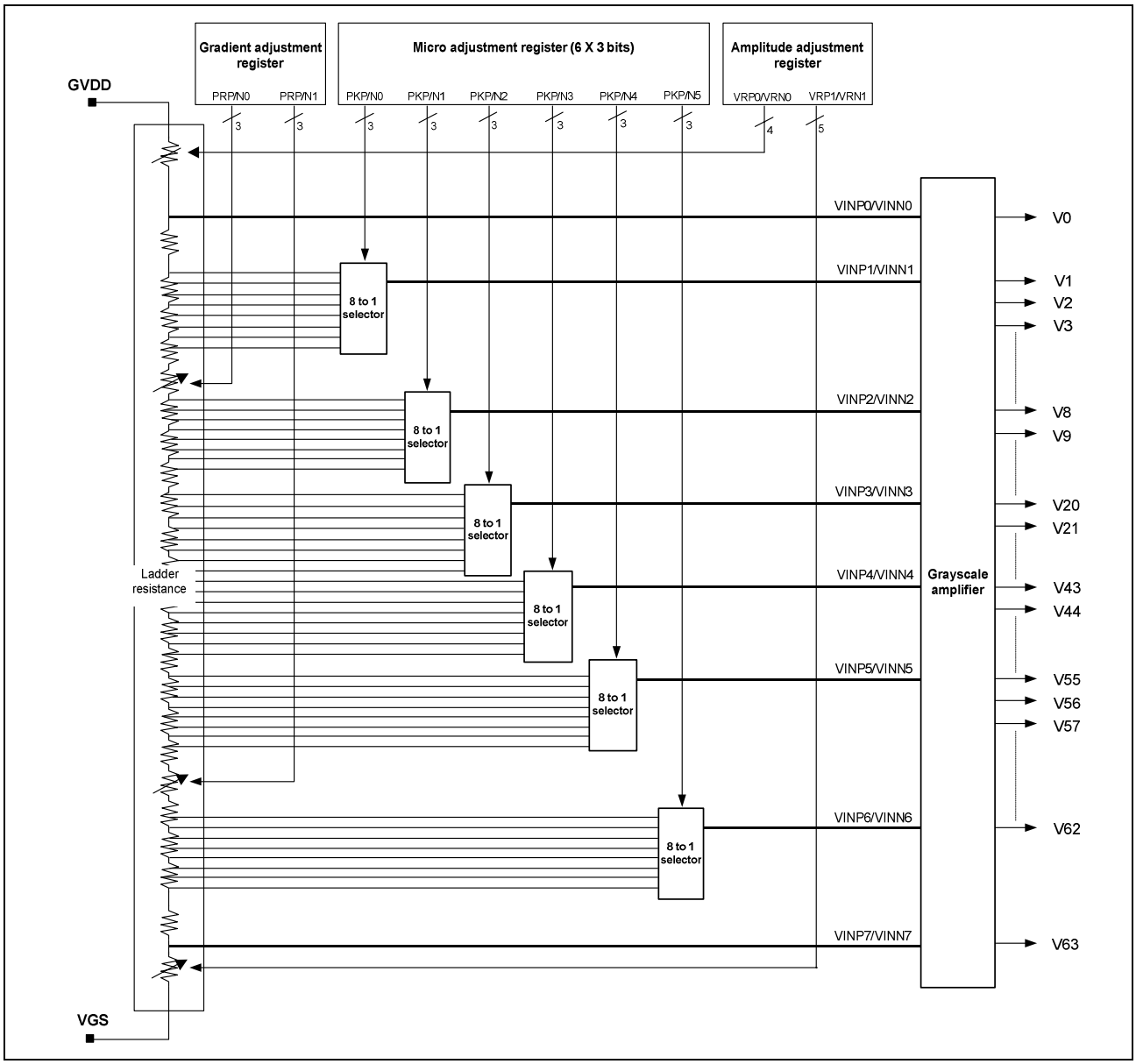


Figure 93. Structure of grayscale amplifier.

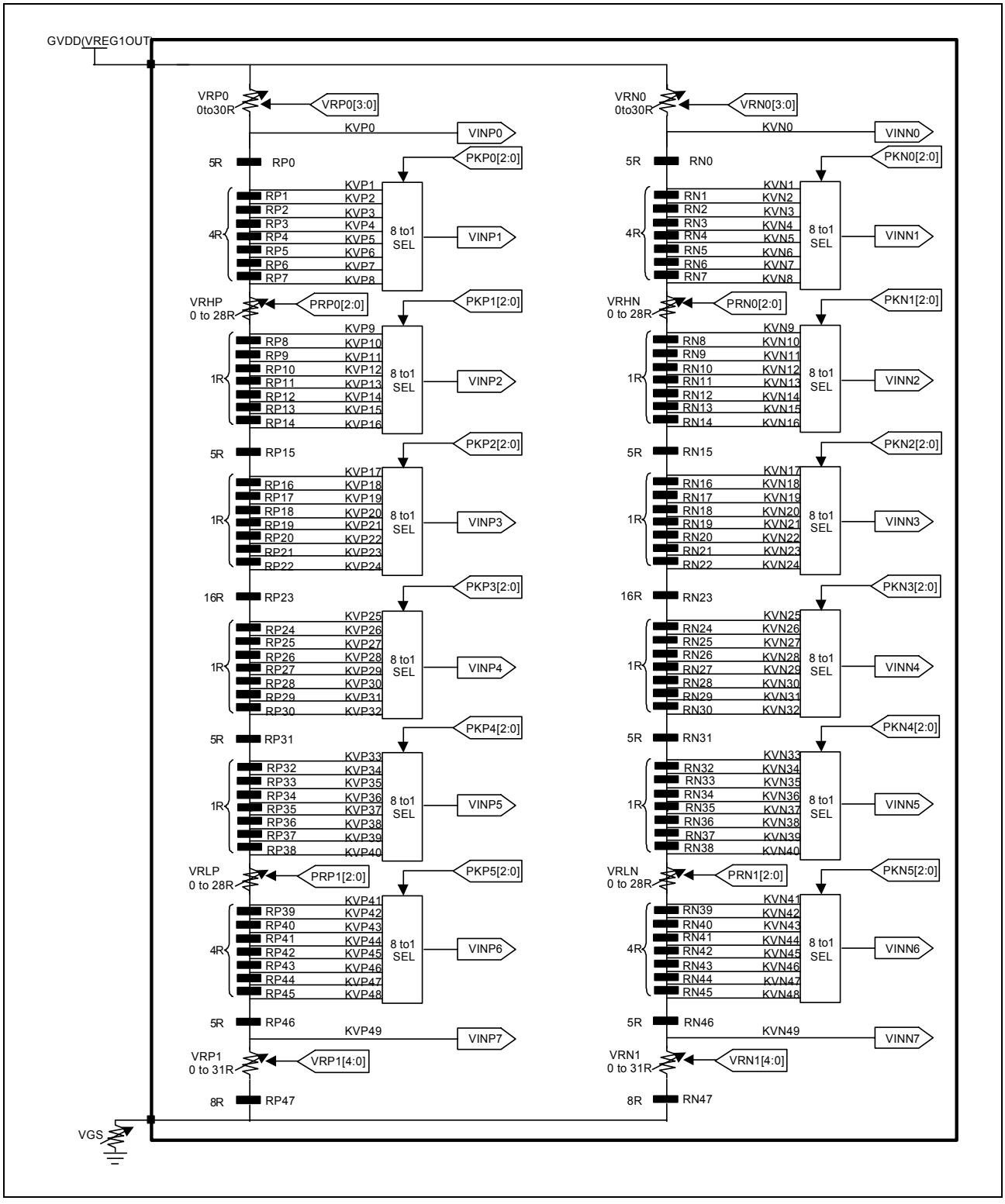


Figure 94. Structure of Ladder / 8 to 1 selector.

11.2. Gamma adjustment register

Gamma adjustment register modifies the gamma curve to comply with the gamma specifications put forth by the LCD panel makers. This register is composed of three sub registers that provide independent means of tuning the gamma curve. The tuning techniques can be categorized into three types – gradient adjustment, amplitude adjustment, and micro-adjustment. Figure 95 shows the effect of the three gamma adjustment techniques on the gamma curve.

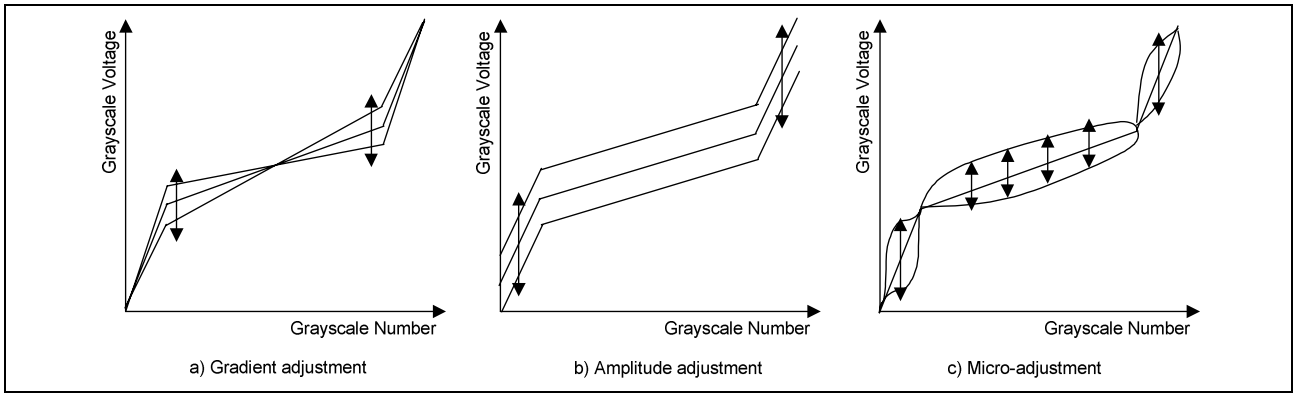


Figure 95. The operation of adjusting register.

11.2.1. Gradient adjustment register

This register is used to shape the gradient in the mid range of the gamma curve without changing its dynamic range. To accomplish this, it controls two variable resistors (VRHP (N), VRLP (N)) within the ladder resistor for grayscale reference voltage generation. The two variable resistors can be controlled independently to allow asymmetric tuning.

11.2.2. Amplitude adjustment register

This register is used to adjust the amplitude of the grayscale voltage This is achieved by controlling the variable resistors, VRP(N)0 and VRP(N)1, located at the top and bottom of the ladder resistor for grayscale reference voltage generation, respectively.

11.2.3. Micro adjustment register

This register is used to fine tune the gamma curve. The fine tuning is accomplished by letting the six 8-to-1 selectors that it controls to select one of the eight voltages coming from the ladder resistor. Refer to Figure 94 for more information.

Table 77. Gamma correction registers.

Register	Positive polarity	Negative polarity	Set-up contents
Gradient adjustment	PRP0[2:0]	PRN0[2:0]	Variable resistor VRHP(N)
	PRP1[2:0]	PRN1[2:0]	Variable resistor VRLP(N)
Amplitude adjustment	VRP0[3:0]	VRN0[3:0]	Variable resistor VRP(N)0
	VRP1[4:0]	VRN1[4:0]	Variable resistor VRP(N)1
Micro-adjustment	PKP0[2:0]	PKN0[2:0]	The voltage of grayscale number 1 is selected by the 8 to 1 selector
	PKP1[2:0]	PKN1[2:0]	The voltage of grayscale number 8 is selected by the 8 to 1 selector
	PKP2[2:0]	PKN2[2:0]	The voltage of grayscale number 20 is selected by the 8 to 1 selector
	PKP3[2:0]	PKN3[2:0]	The voltage of grayscale number 43 is selected by the 8 to 1 selector
	PKP4[2:0]	PKN4[2:0]	The voltage of grayscale number 55 is selected by the 8 to 1 selector
	PKP5[2:0]	PKN5[2:0]	The voltage of grayscale number 62 is selected by the 8 to 1 selector

11.3. Ladder resistor / 8-to-1 selector

This resistor along with the six 8-to-1 selectors, which are controlled by gamma adjustment register, provide the gamma reference voltages for grayscale amplifier. The two ends of the ladder resister string are attached to GVDD and VGS pads.

11.4. Variable resistor

There are two types of variable resistors: One is used for accomplishing gradient adjustment (VRHP (N), VRLP (N)) and for amplitude adjustment (VRP(N)0, VRP(N)1). The resistance values are set by gradient and amplitude adjustment resistors, as shown in Table 75.

Table 78. Gradient Adjustment for the grayscale.

Register value PRP(N) [2:0]	Resistance value VRHP(N)/VRLP(N)
000	0R
001	4R
010	8R
011	12R
100	16R
101	20R
110	24R
111	28R

Table 79. Amplitude Adjustment for the grayscale

Register value VRP(N)0 [3:0]	Resistance value VRP(N)0
0000	0R
0001	2R
0010	4R
. . .	. . .
1101	26R
1110	28R
1111	30R

Table 80. Amplitude Adjustment (2).

Register value VRP(N)1 [4:0] , VR1C=0	Resistance value VRP(N)1
00000	0R
00001	1R
00010	2R
. . .	. . .
11101	29R
11110	30R
11111	31R
Register value VRP(N)1 [4:0] , VR1C=1	**Resistance value VRP(N)1**
00000	0R
00001	2R
00010	4R
. . .	. . .
01101	26R
01110	28R
01111	30R
10000	Not available
. . .	. . .
11101	Not available
11110	Not available
11111	Not available

11.5. 8-to-1 selector

Six 8-to-1 selectors are employed to provide the gamma reference voltages (VIN1-VIN6) to grayscale amplifier. Each selector chooses one of the eight available voltages from the ladder resistor string under the control of micro-adjusting register. Table 78 shows the relationship between the micro-adjusting register and the selecting voltage.

Table 81. Relationship between Micro-adjustment register and selected voltage.

Register value	Selected voltage					
PKP(N) [2:0]	VINP(N)1	VINP(N)2	VINP(N)3	VINP(N)4	VINP(N)5	VINP(N)6
000	KVP(N)1	KVP(N)9	KVP(N)17	KVP(N)25	KVP(N)33	KVP(N)41
001	KVP(N)2	KVP(N)10	KVP(N)18	KVP(N)26	KVP(N)34	KVP(N)42
010	KVP(N)3	KVP(N)11	KVP(N)19	KVP(N)27	KVP(N)35	KVP(N)43
011	KVP(N)4	KVP(N)12	KVP(N)20	KVP(N)28	KVP(N)36	KVP(N)44
100	KVP(N)5	KVP(N)13	KVP(N)21	KVP(N)29	KVP(N)37	KVP(N)45
101	KVP(N)6	KVP(N)14	KVP(N)22	KVP(N)30	KVP(N)38	KVP(N)46
110	KVP(N)7	KVP(N)15	KVP(N)23	KVP(N)31	KVP(N)39	KVP(N)47
111	KVP(N)8	KVP(N)16	KVP(N)24	KVP(N)32	KVP(N)40	KVP(N)48

Table 82. Gamma Adjusting Voltage Formula (Positive polarity) I.

Pins	Formula	Micro-adjusting register value	Reference voltage
KVP0	GVDD - ΔV *VRP0 / SUMRP	-	VINP0
KVP1	GVDD - ΔV * (VRP0 + 5R) / SUMRP	PKP0[2:0] = 000	VINP1
KVP2	GVDD - ΔV * (VRP0 + 9R) / SUMRP	PKP0[2:0] = 001	
KVP3	GVDD - ΔV * (VRP0 + 13R) / SUMRP	PKP0[2:0] = 010	
KVP4	GVDD - ΔV * (VRP0 + 17R) / SUMRP	PKP0[2:0] = 011	
KVP5	GVDD - ΔV * (VRP0 + 21R) / SUMRP	PKP0[2:0] = 100	
KVP6	GVDD - ΔV * (VRP0 + 25R) / SUMRP	PKP0[2:0] = 101	
KVP7	GVDD - ΔV * (VRP0 + 29R) / SUMRP	PKP0[2:0] = 110	
KVP8	GVDD - ΔV * (VRP0 + 33R) / SUMRP	PKP0[2:0] = 111	
KVP9	GVDD - ΔV * (VRP0 + 33R + VRHP) / SUMRP	PKP1[2:0] = 000	VINP2
KVP10	GVDD - ΔV * (VRP0 + 34R + VRHP) / SUMRP	PKP1[2:0] = 001	
KVP11	GVDD - ΔV * (VRP0 + 35R + VRHP) / SUMRP	PKP1[2:0] = 010	
KVP12	GVDD - ΔV * (VRP0 + 36R + VRHP) / SUMRP	PKP1[2:0] = 011	
KVP13	GVDD - ΔV * (VRP0 + 37R + VRHP) / SUMRP	PKP1[2:0] = 100	
KVP14	GVDD - ΔV * (VRP0 + 38R + VRHP) / SUMRP	PKP1[2:0] = 101	
KVP15	GVDD - ΔV * (VRP0 + 39R + VRHP) / SUMRP	PKP1[2:0] = 110	
KVP16	GVDD - ΔV * (VRP0 + 40R + VRHP) / SUMRP	PKP1[2:0] = 111	
KVP17	GVDD - ΔV * (VRP0 + 45R + VRHP) / SUMRP	PKP2[2:0] = 000	VINP3
KVP18	GVDD - ΔV * (VRP0 + 46R + VRHP) / SUMRP	PKP2[2:0] = 001	
KVP19	GVDD - ΔV * (VRP0 + 47R + VRHP) / SUMRP	PKP2[2:0] = 010	
KVP20	GVDD - ΔV * (VRP0 + 48R + VRHP) / SUMRP	PKP2[2:0] = 011	
KVP21	GVDD - ΔV * (VRP0 + 49R + VRHP) / SUMRP	PKP2[2:0] = 100	
KVP22	GVDD - ΔV * (VRP0 + 50R + VRHP) / SUMRP	PKP2[2:0] = 101	
KVP23	GVDD - ΔV * (VRP0 + 51R + VRHP) / SUMRP	PKP2[2:0] = 110	
KVP24	GVDD - ΔV * (VRP0 + 52R + VRHP) / SUMRP	PKP2[2:0] = 111	
KVP25	GVDD - ΔV * (VRP0 + 68R + VRHP) / SUMRP	PKP3[2:0] = 000	VINP4
KVP26	GVDD - ΔV * (VRP0 + 69R + VRHP) / SUMRP	PKP3[2:0] = 001	
KVP27	GVDD - ΔV * (VRP0 + 70R + VRHP) / SUMRP	PKP3[2:0] = 010	
KVP28	GVDD - ΔV * (VRP0 + 71R + VRHP) / SUMRP	PKP3[2:0] = 011	
KVP29	GVDD - ΔV * (VRP0 + 72R + VRHP) / SUMRP	PKP3[2:0] = 100	
KVP30	GVDD - ΔV * (VRP0 + 73R + VRHP) / SUMRP	PKP3[2:0] = 101	
KVP31	GVDD - ΔV * (VRP0 + 74R + VRHP) / SUMRP	PKP3[2:0] = 110	
KVP32	GVDD - ΔV * (VRP0 + 75R + VRHP) / SUMRP	PKP3[2:0] = 111	
KVP33	GVDD - ΔV * (VRP0 + 80R + VRHP) / SUMRP	PKP4[2:0] = 000	VINP5
KVP34	GVDD - ΔV * (VRP0 + 81R + VRHP) / SUMRP	PKP4[2:0] = 001	
KVP35	GVDD - ΔV * (VRP0 + 82R + VRHP) / SUMRP	PKP4[2:0] = 010	
KVP36	GVDD - ΔV * (VRP0 + 83R + VRHP) / SUMRP	PKP4[2:0] = 011	
KVP37	GVDD - ΔV * (VRP0 + 84R + VRHP) / SUMRP	PKP4[2:0] = 100	
KVP38	GVDD - ΔV * (VRP0 + 85R + VRHP) / SUMRP	PKP4[2:0] = 101	
KVP39	GVDD - ΔV * (VRP0 + 86R + VRHP) / SUMRP	PKP4[2:0] = 110	
KVP40	GVDD - ΔV * (VRP0 + 87R + VRHP) / SUMRP	PKP4[2:0] = 111	
KVP41	GVDD - ΔV * (VRP0 + 87R + VRHP + VRLP) / SUMRP	PKP5[2:0] = 000	VINP6
KVP42	GVDD - ΔV * (VRP0 + 91R + VRHP + VRLP) / SUMRP	PKP5[2:0] = 001	
KVP43	GVDD - ΔV * (VRP0 + 95R + VRHP + VRLP) / SUMRP	PKP5[2:0] = 010	
KVP44	GVDD - ΔV * (VRP0 + 99R + VRHP + VRLP) / SUMRP	PKP5[2:0] = 011	
KVP45	GVDD - ΔV * (VRP0 + 103R + VRHP + VRLP) / SUMRP	PKP5[2:0] = 100	
KVP46	GVDD - ΔV * (VRP0 + 107R + VRHP + VRLP) / SUMRP	PKP5[2:0] = 101	
KVP47	GVDD - ΔV * (VRP0 + 111R + VRHP + VRLP) / SUMRP	PKP5[2:0] = 110	
KVP48	GVDD - ΔV * (VRP0 + 115R + VRHP + VRLP) / SUMRP	PKP5[2:0] = 111	
KVP49	GVDD - ΔV * (VRP0 + 120R + VRHP + VRLP) / SUMRP	-	VINP7

SUMRP: The total of the positive polarity ladder resistance = 128R + VRHP + VRLP + VRP0+VRP1

ΔV: Potential difference between GVDD-VGS

Table 83. Gamma Voltage Formula (Positive Polarity) II.

Grayscale voltage	Formula	Grayscale voltage	Formula
V0	VINP0	V32	V20-(V20-V43)*(12/23)
V1	VINP1	V33	V20-(V20-V43)*(13/23)
V2	V1-(V1-V8)*(28/96)	V34	V20-(V20-V43)*(14/23)
V3	V1-(V1-V8)*(42/96)	V35	V20-(V20-V43)*(15/23)
V4	V1-(V1-V8)*(60/96)	V36	V20-(V20-V43)*(16/23)
V5	V1-(V1-V8)*(69/96)	V37	V20-(V20-V43)*(17/23)
V6	V1-(V1-V8)*(78/96)	V38	V20-(V20-V43)*(18/23)
V7	V1-(V1-V8)*(87/96)	V39	V20-(V20-V43)*(19/23)
V8	VINP2	V40	V20-(V20-V43)*(20/23)
V9	V8-(V8-V20)*(2/24)	V41	V20-(V20-V43)*(21/23)
V10	V8-(V8-V20)*(4/24)	V42	V20-(V20-V43)*(22/23)
V11	V8-(V8-V20)*(6/24)	V43	VINP4
V12	V8-(V8-V20)*(8/24)	V44	V43-(V43-V55)*(2/24)
V13	V8-(V8-V20)*(10/24)	V45	V43-(V43-V55)*(4/24)
V14	V8-(V8-V20)*(12/24)	V46	V43-(V43-V55)*(6/24)
V15	V8-(V8-V20)*(14/24)	V47	V43-(V43-V55)*(8/24)
V16	V8-(V8-V20)*(16/24)	V48	V43-(V43-V55)*(10/24)
V17	V8-(V8-V20)*(18/24)	V49	V43-(V43-V55)*(12/24)
V18	V8-(V8-V20)*(20/24)	V50	V43-(V43-V55)*(14/24)
V19	V8-(V8-V20)*(22/24)	V51	V43-(V43-V55)*(16/24)
V20	VINP3	V52	V43-(V43-V55)*(18/24)
V21	V20-(V20-V43)*(1/23)	V53	V43-(V43-V55)*(20/24)
V22	V20-(V20-V43)*(2/23)	V54	V43-(V43-V55)*(22/24)
V23	V20-(V20-V43)*(3/23)	V55	VINP5
V24	V20-(V20-V43)*(4/23)	V56	V55-(V55-V62)*(9/96)
V25	V20-(V20-V43)*(5/23)	V57	V55-(V55-V62)*(18/96)
V26	V20-(V20-V43)*(6/23)	V58	V55-(V55-V62)*(27/96)
V27	V20-(V20-V43)*(7/23)	V59	V55-(V55-V62)*(36/96)
V28	V20-(V20-V43)*(8/23)	V60	V55-(V55-V62)*(54/96)
V29	V20-(V20-V43)*(9/23)	V61	V55-(V55-V62)*(68/96)
V30	V20-(V20-V43)*(10/23)	V62	VINP6
V31	V20-(V20-V43)*(11/23)	V63	VINP7

[Note]

Keep the following conditions.

AVDD – V0 > 0.5V

AVDD – V8 > 1.1V

Table 84. Gamma Adjusting Voltage Formula (Negative polarity) 1

Pins	Formula	Micro-adjusting register value	Reference voltage
KVN0	GVDD - ΔV *VRN0 / SUMRN	-	VINN0
KVN1	GVDD - ΔV * (VRN0 + 5R) / SUMRN	PKN0[2:0] = 000	VINN1
KVN2	GVDD - ΔV * (VRN0 + 9R) / SUMRN	PKN0[2:0] = 001	
KVN3	GVDD - ΔV * (VRN0 + 13R) / SUMRN	PKN0[2:0] = 010	
KVN4	GVDD - ΔV * (VRN0 + 17R) / SUMRN	PKN0[2:0] = 011	
KVN5	GVDD - ΔV * (VRN0 + 21R) / SUMRN	PKN0[2:0] = 100	
KVN6	GVDD - ΔV * (VRN0 + 25R) / SUMRN	PKN0[2:0] = 101	
KVN7	GVDD - ΔV * (VRN0 + 29R) / SUMRN	PKN0[2:0] = 110	
KVN8	GVDD - ΔV * (VRN0 + 33R) / SUMRN	PKN0[2:0] = 111	
KVN9	GVDD - ΔV * (VRN0 + 33R + VRHN) / SUMRN	PKN1[2:0] = 000	VINN2
KVN10	GVDD - ΔV * (VRN0 + 34R + VRHN) / SUMRN	PKN1[2:0] = 001	
KVN11	GVDD - ΔV * (VRN0 + 35R + VRHN) / SUMRN	PKN1[2:0] = 010	
KVN12	GVDD - ΔV * (VRN0 + 36R + VRHN) / SUMRN	PKN1[2:0] = 011	
KVN13	GVDD - ΔV * (VRN0 + 37R + VRHN) / SUMRN	PKN1[2:0] = 100	
KVN14	GVDD - ΔV * (VRN0 + 38R + VRHN) / SUMRN	PKN1[2:0] = 101	
KVN15	GVDD - ΔV * (VRN0 + 39R + VRHN) / SUMRN	PKN1[2:0] = 110	
KVN16	GVDD - ΔV * (VRN0 + 40R + VRHN) / SUMRN	PKN1[2:0] = 111	
KVN17	GVDD - ΔV * (VRN0 + 45R + VRHN) / SUMRN	PKN2[2:0] = 000	VINN3
KVN18	GVDD - ΔV * (VRN0 + 46R + VRHN) / SUMRN	PKN2[2:0] = 001	
KVN19	GVDD - ΔV * (VRN0 + 47R + VRHN) / SUMRN	PKN2[2:0] = 010	
KVN20	GVDD - ΔV * (VRN0 + 48R + VRHN) / SUMRN	PKN2[2:0] = 011	
KVN21	GVDD - ΔV * (VRN0 + 49R + VRHN) / SUMRN	PKN2[2:0] = 100	
KVN22	GVDD - ΔV * (VRN0 + 50R + VRHN) / SUMRN	PKN2[2:0] = 101	
KVN23	GVDD - ΔV * (VRN0 + 51R + VRHN) / SUMRN	PKN2[2:0] = 110	
KVN24	GVDD - ΔV * (VRN0 + 52R + VRHN) / SUMRN	PKN2[2:0] = 111	
KVN25	GVDD - ΔV * (VRN0 + 68R + VRHN) / SUMRN	PKN3[2:0] = 000	VINN4
KVN26	GVDD - ΔV * (VRN0 + 69R + VRHN) / SUMRN	PKN3[2:0] = 001	
KVN27	GVDD - ΔV * (VRN0 + 70R + VRHN) / SUMRN	PKN3[2:0] = 010	
KVN28	GVDD - ΔV * (VRN0 + 71R + VRHN) / SUMRN	PKN3[2:0] = 011	
KVN29	GVDD - ΔV * (VRN0 + 72R + VRHN) / SUMRN	PKN3[2:0] = 100	
KVN30	GVDD - ΔV * (VRN0 + 73R + VRHN) / SUMRN	PKN3[2:0] = 101	
KVN31	GVDD - ΔV * (VRN0 + 74R + VRHN) / SUMRN	PKN3[2:0] = 110	
KVN32	GVDD - ΔV * (VRN0 + 75R + VRHN) / SUMRN	PKN3[2:0] = 111	
KVN33	GVDD - ΔV * (VRN0 + 80R + VRHN) / SUMRN	PKN4[2:0] = 000	VINN5
KVN34	GVDD - ΔV * (VRN0 + 81R + VRHN) / SUMRN	PKN4[2:0] = 001	
KVN35	GVDD - ΔV * (VRN0 + 82R + VRHN) / SUMRN	PKN4[2:0] = 010	
KVN36	GVDD - ΔV * (VRN0 + 83R + VRHN) / SUMRN	PKN4[2:0] = 011	
KVN37	GVDD - ΔV * (VRN0 + 84R + VRHN) / SUMRN	PKN4[2:0] = 100	
KVN38	GVDD - ΔV * (VRN0 + 85R + VRHN) / SUMRN	PKN4[2:0] = 101	
KVN39	GVDD - ΔV * (VRN0 + 86R + VRHN) / SUMRN	PKN4[2:0] = 110	
KVN40	GVDD - ΔV * (VRN0 + 87R + VRHN) / SUMRN	PKN4[2:0] = 111	
KVN41	GVDD - ΔV * (VRN0 + 87R + VRHN + VRLN) / SUMRN	PKN5[2:0] = 000	VINN6
KVN42	GVDD - ΔV * (VRN0 + 91R + VRHN + VRLN) / SUMRN	PKN5[2:0] = 001	
KVN43	GVDD - ΔV * (VRN0 + 95R + VRHN + VRLN) / SUMRN	PKN5[2:0] = 010	
KVN44	GVDD - ΔV * (VRN0 + 99R + VRHN + VRLN) / SUMRN	PKN5[2:0] = 011	
KVN45	GVDD - ΔV * (VRN0 + 103R + VRHN + VRLN) / SUMRN	PKN5[2:0] = 100	
KVN46	GVDD - ΔV * (VRN0 + 107R + VRHN + VRLN) / SUMRN	PKN5[2:0] = 101	
KVN47	GVDD - ΔV * (VRN0 + 111R + VRHN + VRLN) / SUMRN	PKN5[2:0] = 110	
KVN48	GVDD - ΔV * (VRN0 + 115R + VRHN + VRLN) / SUMRN	PKN5[2:0] = 111	
KVN49	GVDD - ΔV * (VRN0 + 120R + VRHN + VRLN) / SUMRN	-	VINN7

SUMRN: The total of the negative polarity ladder resistance = 128R + VRHN + VRLN + VRN0+VRN1
ΔV: Potential difference between GVDD-VGS

Table 85. Gamma Voltage Formula (Negative Polarity) 2

Grayscale voltage	Formula	Grayscale voltage	Formula
V0	VINN0	V32	V20-(V20-V43)*(12/23)
V1	VINN1	V33	V20-(V20-V43)*(13/23)
V2	V1-(V1-V8)*(28/96)	V34	V20-(V20-V43)*(14/23)
V3	V1-(V1-V8)*(42/96)	V35	V20-(V20-V43)*(15/23)
V4	V1-(V1-V8)*(60/96)	V36	V20-(V20-V43)*(16/23)
V5	V1-(V1-V8)*(69/96)	V37	V20-(V20-V43)*(17/23)
V6	V1-(V1-V8)*(78/96)	V38	V20-(V20-V43)*(18/23)
V7	V1-(V1-V8)*(87/96)	V39	V20-(V20-V43)*(19/23)
V8	VINN2	V40	V20-(V20-V43)*(20/23)
V9	V8-(V8-V20)*(2/24)	V41	V20-(V20-V43)*(21/23)
V10	V8-(V8-V20)*(4/24)	V42	V20-(V20-V43)*(22/23)
V11	V8-(V8-V20)*(6/24)	V43	VINN4
V12	V8-(V8-V20)*(8/24)	V44	V43-(V43-V55)*(2/24)
V13	V8-(V8-V20)*(10/24)	V45	V43-(V43-V55)*(4/24)
V14	V8-(V8-V20)*(12/24)	V46	V43-(V43-V55)*(6/24)
V15	V8-(V8-V20)*(14/24)	V47	V43-(V43-V55)*(8/24)
V16	V8-(V8-V20)*(16/24)	V48	V43-(V43-V55)*(10/24)
V17	V8-(V8-V20)*(18/24)	V49	V43-(V43-V55)*(12/24)
V18	V8-(V8-V20)*(20/24)	V50	V43-(V43-V55)*(14/24)
V19	V8-(V8-V20)*(22/24)	V51	V43-(V43-V55)*(16/24)
V20	VINN3	V52	V43-(V43-V55)*(18/24)
V21	V20-(V20-V43)*(1/23)	V53	V43-(V43-V55)*(20/24)
V22	V20-(V20-V43)*(2/23)	V54	V43-(V43-V55)*(22/24)
V23	V20-(V20-V43)*(3/23)	V55	VINN5
V24	V20-(V20-V43)*(4/23)	V56	V55-(V55-V62)*(9/96)
V25	V20-(V20-V43)*(5/23)	V57	V55-(V55-V62)*(18/96)
V26	V20-(V20-V43)*(6/23)	V58	V55-(V55-V62)*(27/96)
V27	V20-(V20-V43)*(7/23)	V59	V55-(V55-V62)*(36/96)
V28	V20-(V20-V43)*(8/23)	V60	V55-(V55-V62)*(54/96)
V29	V20-(V20-V43)*(9/23)	V61	V55-(V55-V62)*(68/96)
V30	V20-(V20-V43)*(10/23)	V62	VINN6
V31	V20-(V20-V43)*(11/23)	V63	VINN7

[Note]

Keep the following conditions.

AVDD – V0 > 0.5V

AVDD – V8 > 1.1V

11.6. Output level of a source driver as a function of GRAM data

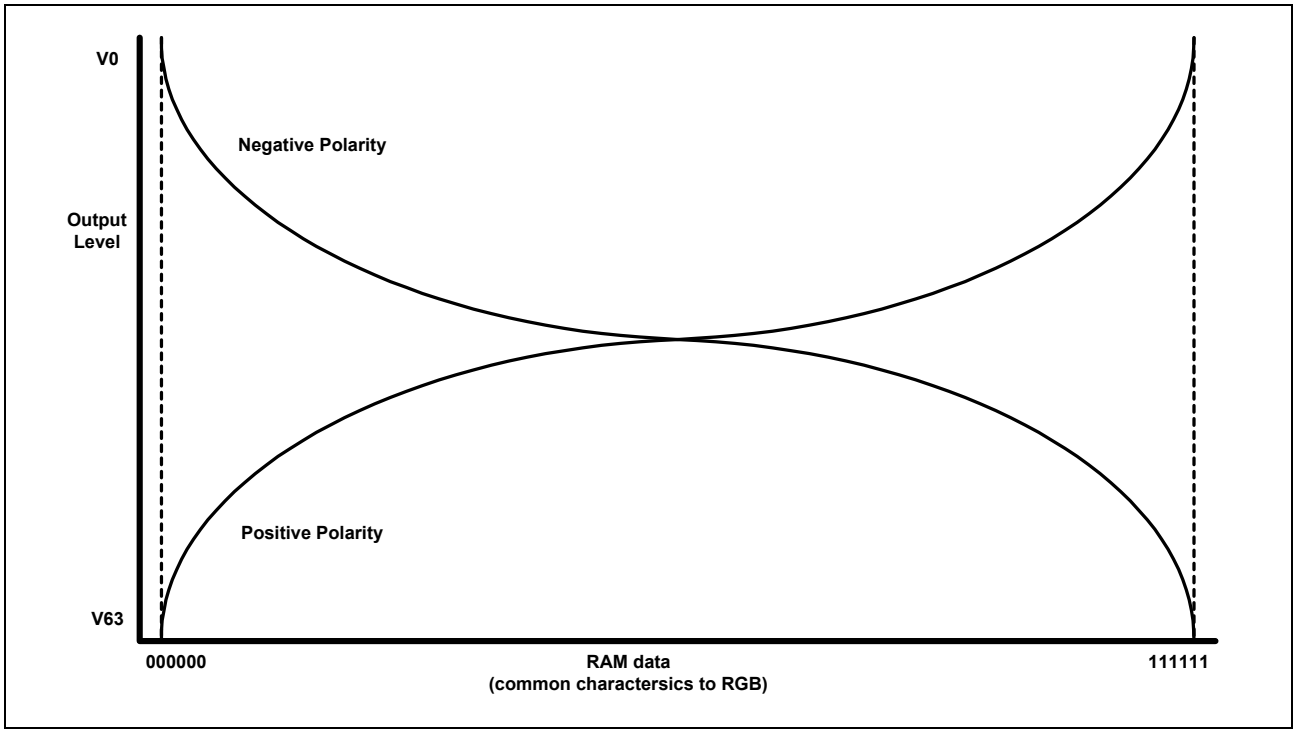
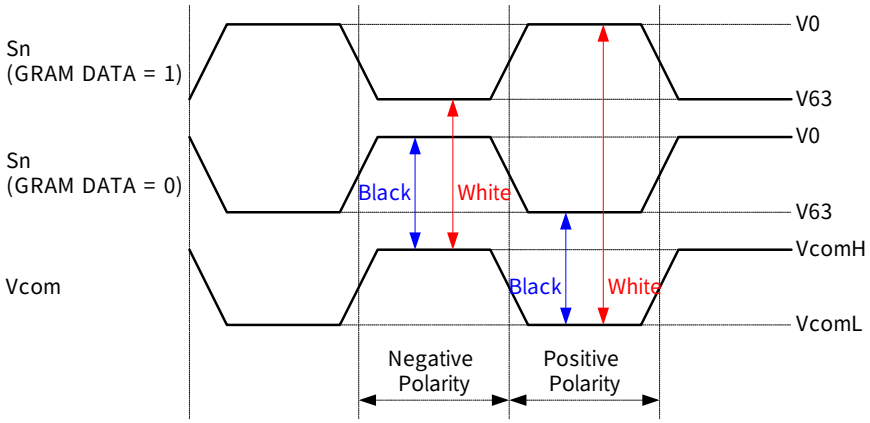
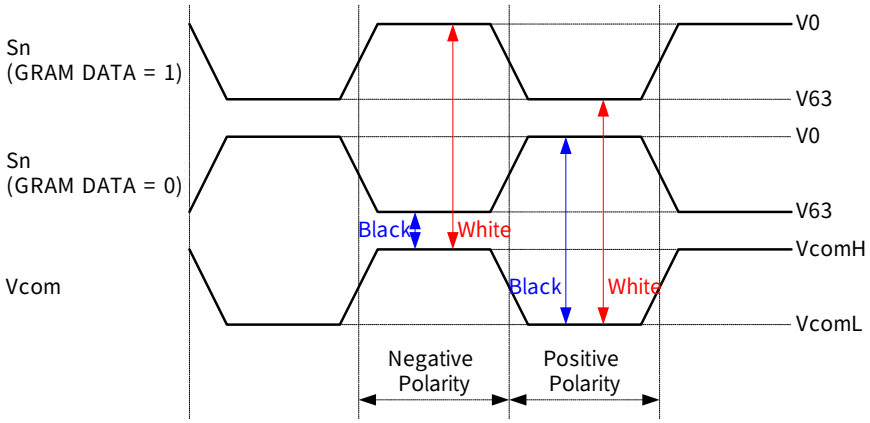


Figure 96. Relationship between RAM data and output voltage



(a) For Normally Black Panel (REV = 0)



(b) For Normally White Panel (REV = 1)

Figure 97. Relationship between source output and Vcom.

12. 8-color display mode

An 8-color display mode is also provided by the S6D0151. In an 8-color mode of operation, gray scale voltage generation (V0-V63) is halted to conserve power and the values of gamma micro-adjustment registers (PKP and PKN) become invalid. Also, RGB data in GRAM should be set to either 000000 or 111111.

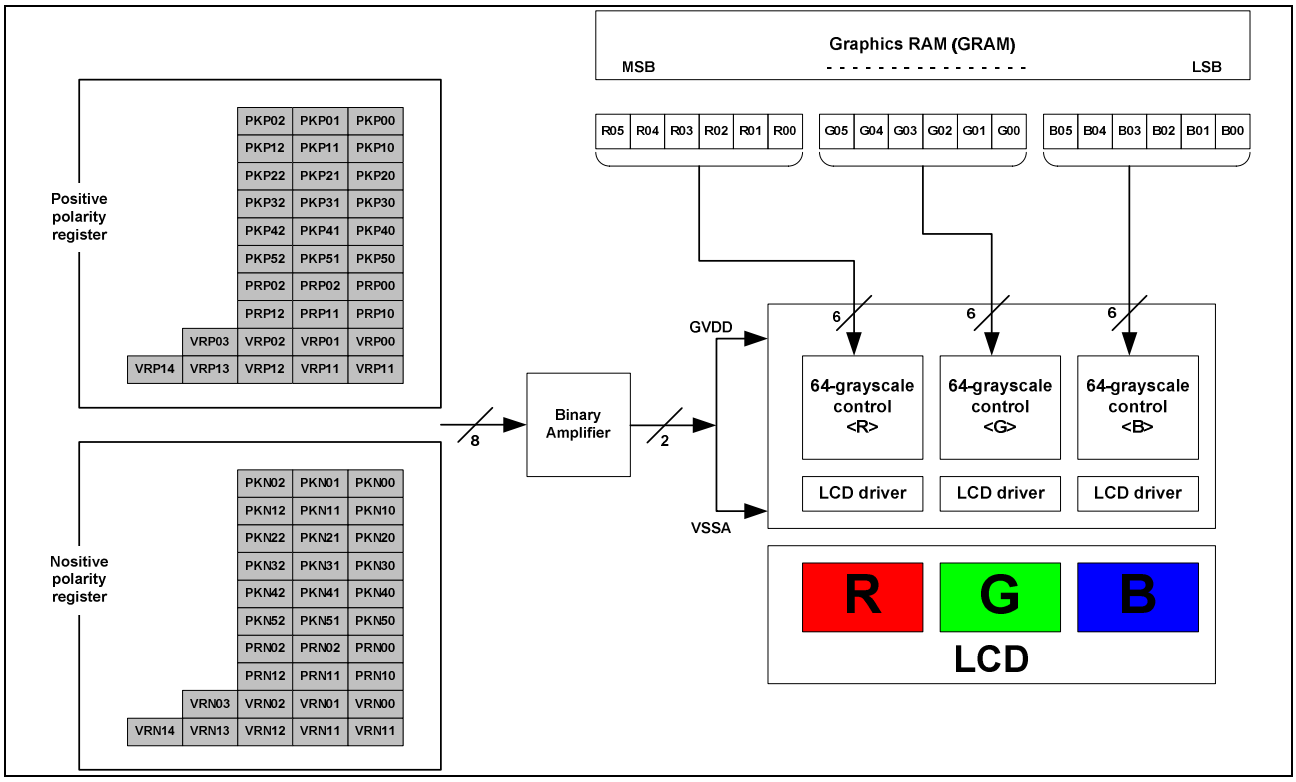


Figure 98. 8-color display control.

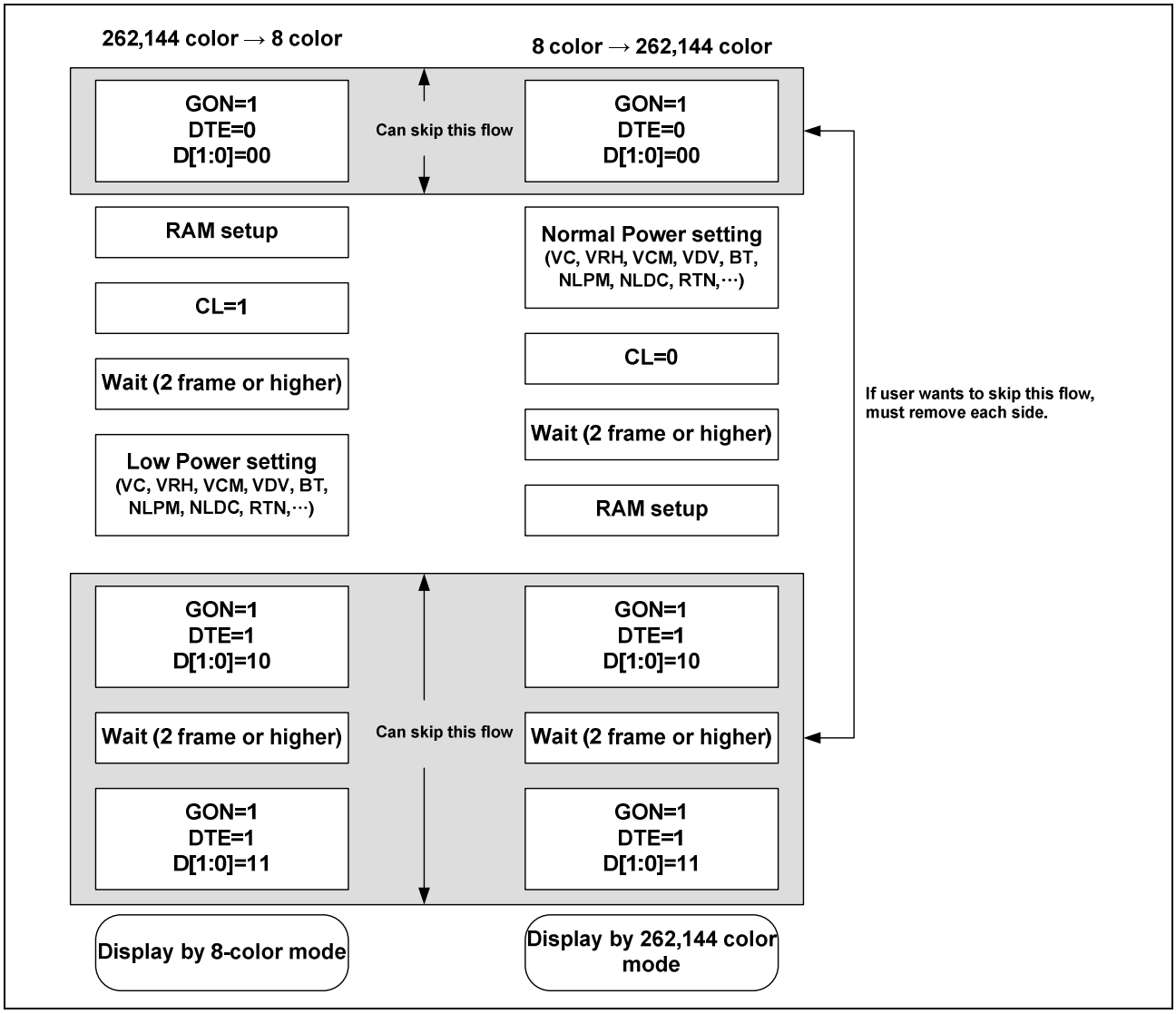


Figure 99. Set up procedure for the 8-color mode.

13. Instruction setup flow

13.1. Display ON / OFF sequence

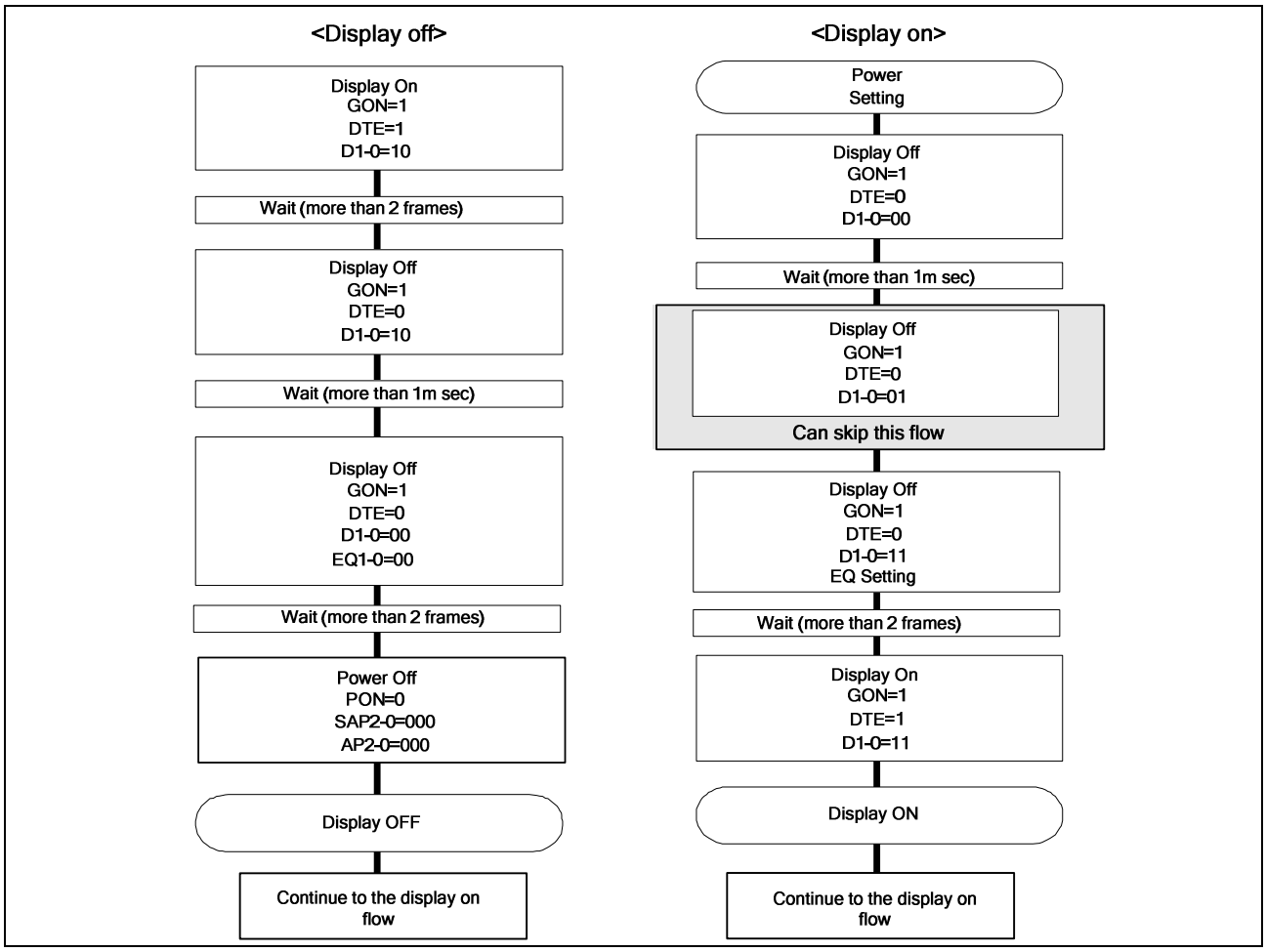


Figure 100. Display ON / OFF sequence.

13.2. Standby / sleep sequence

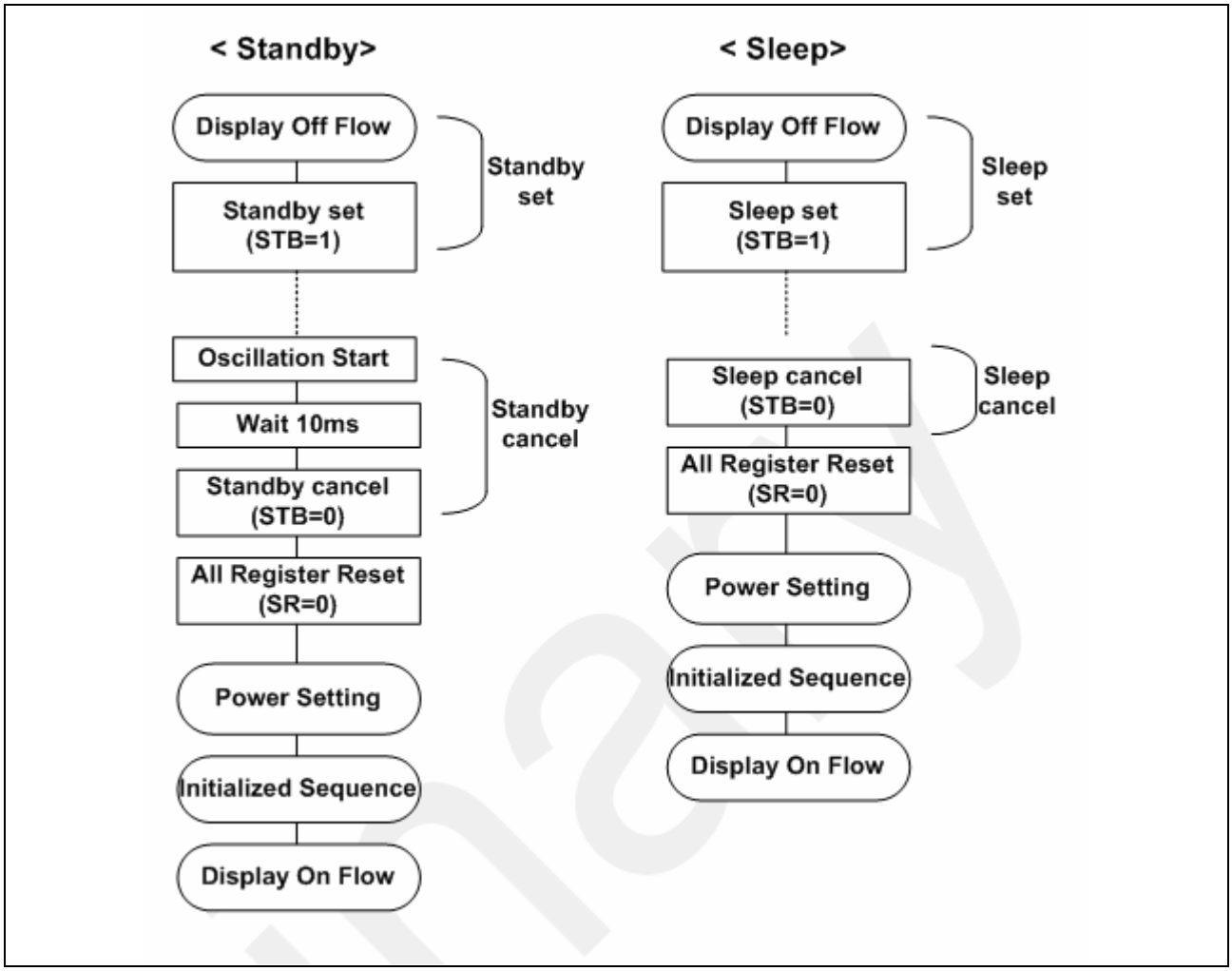


Figure 101. Standby/sleep sequence.

14. Oscillation circuit

A fully integrated R-C oscillator in the S6D0151 requires no external resistor. Its oscillation frequency can be programmed through oscillator frequency control register. To conserve power the oscillator stops operating in the standby mode.

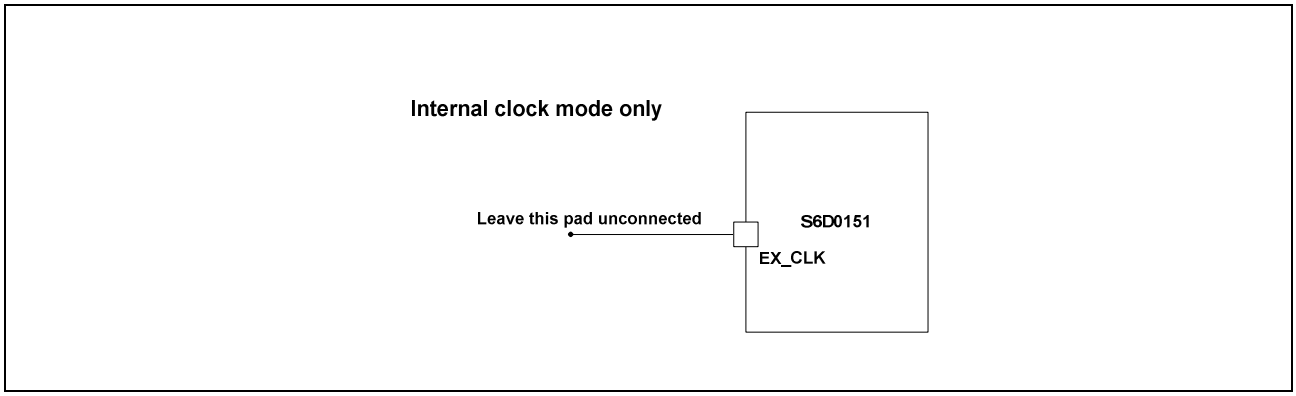


Figure 102. Oscillator Circuit.

15. Application circuit

15.1. Typcial application circuit

A typical application circuit is shown in following figure.

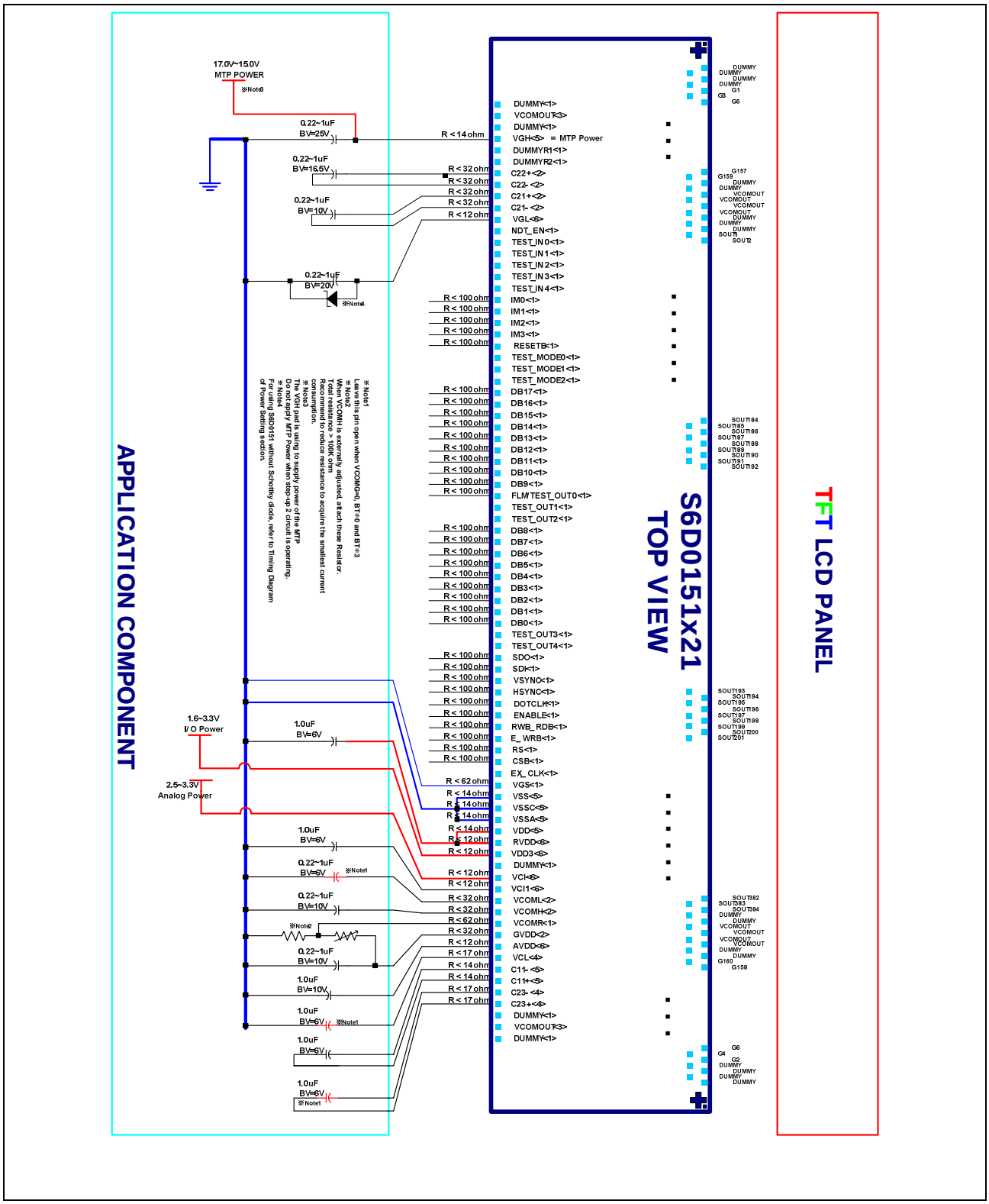


Figure 103. Application Circuit.

15.2. External component

Table 86. External component

Name	Device	Value	Connection	Note	
C1	Capacitor	1uF	VCI1 - GND		6V
C2	Capacitor	1uF	AVDD – GND		10V
C3	Capacitor	0.22 ~ 1uF	VGH – GND		25V
C4	Capacitor	0.22 ~ 1uF	VGL – GND		20V
C5	Capacitor	0.22 ~ 1uF	GVDD – GND		10V
C6	Capacitor	0.22 ~ 1uF	VCOMH - GND	Maximum	10V
C7	Capacitor	0.22 ~ 1uF	VCOML – GND	Ratings	6V
C8	Capacitor	1uF	C11+ – C11-	Voltage	6V
C9	Capacitor	0.22 ~ 1uF	C21+ – C21-		10V
C10	Capacitor	0.22 ~ 1uF	C22+ – C22-		16.5V
C11	Capacitor	1uF	C23+ – C23-		6V
C12	Capacitor	1uF	VCL-GND		6V
C13	Capacitor	1uF	RVDD – GND		6V
D1	Diode	-	(+)VGL – GND(-)	VF < 0.4V (@ IF = 20mA, Ta = 25°C) VR ≥ max.25V	